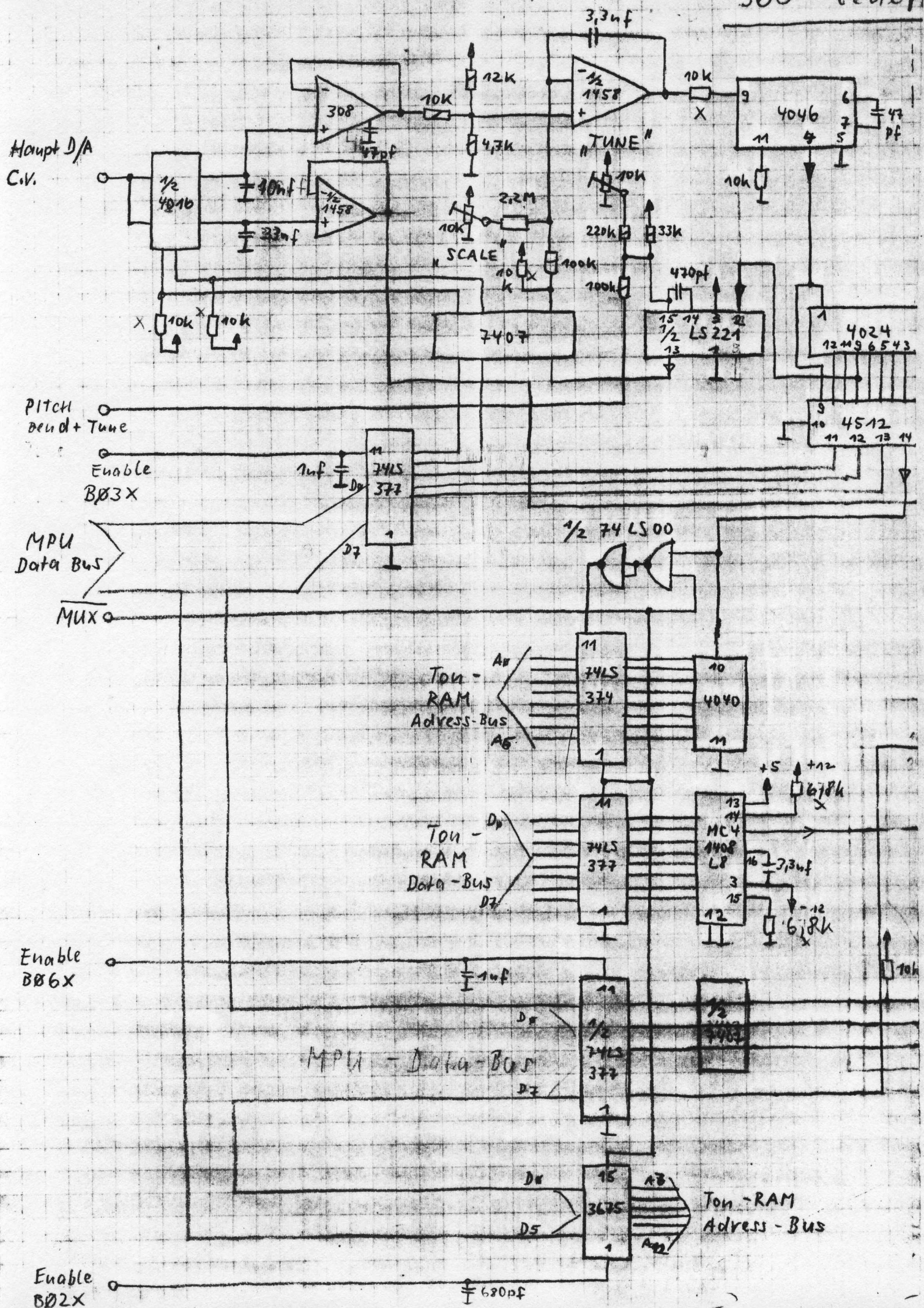
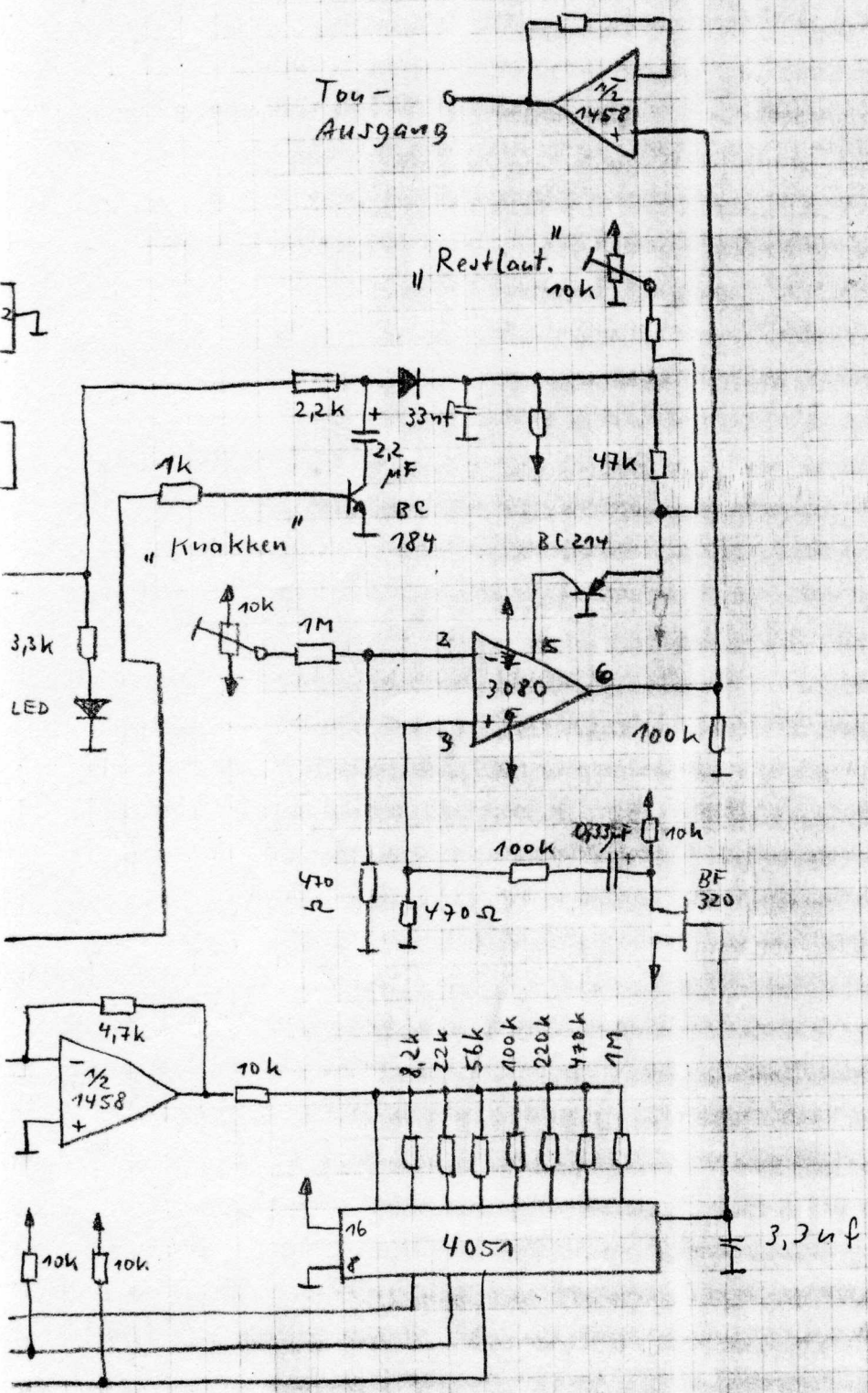




ador 1/2 platine



360A

"ANIN" auf 1/0 Board Dil Buche

Stecker "Analog Inputs"

Analog Ext.

	360	340	
1 GND	16 +	+	
2 GND	1 Pitch Bend	P.L.	
3 "A"	15 GND	GND	
4 Fine Tune C.V. → 7(10)	2 GND	GND	
5	14 Mod. FR		
6	3 +		
7 Select A	13 GND	GND	
8 14h. 9-16	Y Fine Tune	Fine Tune	Manual
	12 +	+	
9 Select C	5 DMS	DMS	→ Ch3
10 Select B	11 DMS	DMS	
11 14h. 1-8			
12 GND	6	PWN C.V.	Ch2
13 +12V	10 +		
14 Trigger in = R - Reset	7 Ext. C.V.	Ext C.V. 1 = Ch. 0	
15 -12V	9 x - Anin	Ext. C.V. 2 = Ch. 1	
16 Komp. out = K	8 GND		

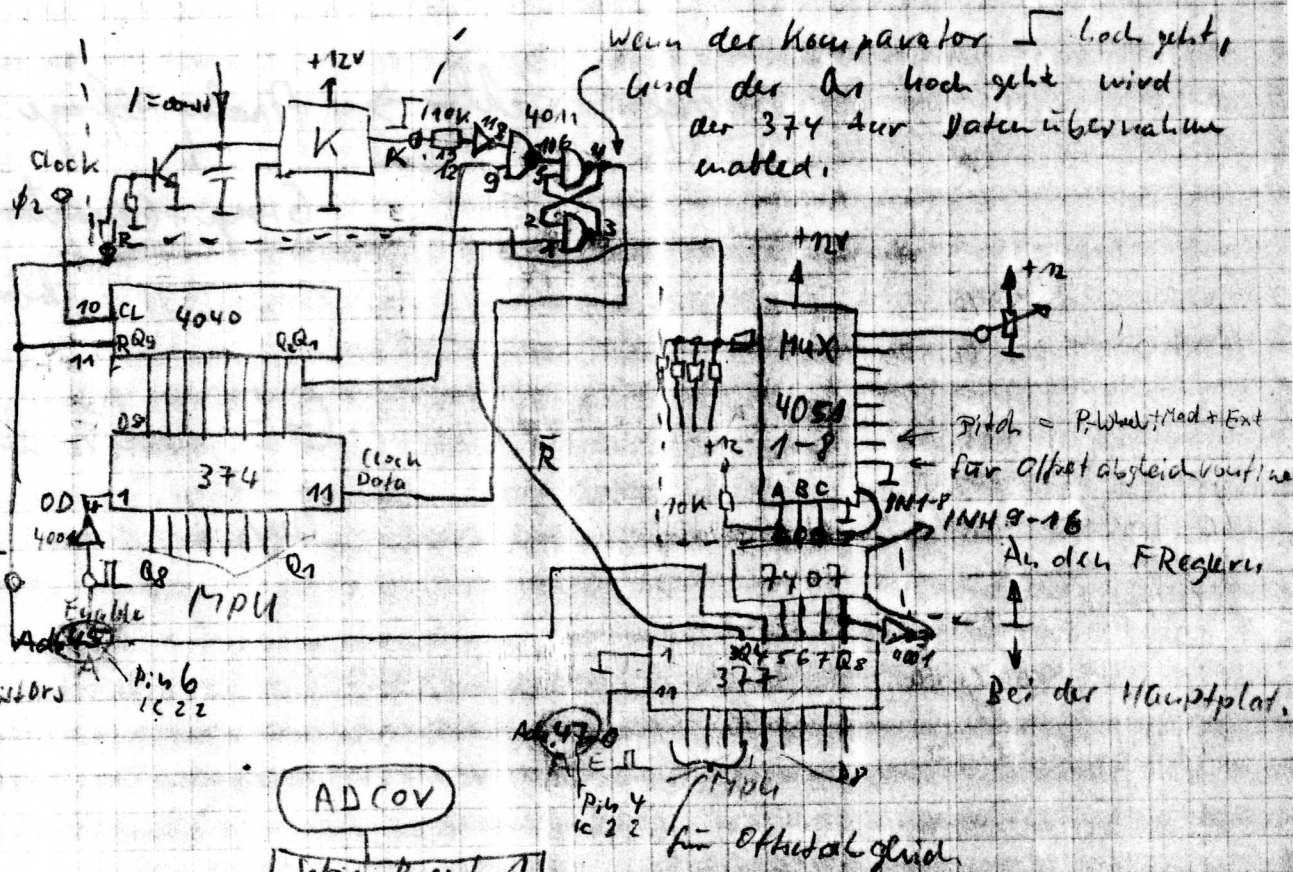
Eingänge Decodierung:

- 0 = Speed
- 1 = Delay
- 2 = Transforms
- 3 = Attack
- 4 Peak
- 5 VCA Decay
- 6 VCA Attack
- 7 (Pitch Bend) Dyn.
- 8 - Decay

- 9 Sustain
- 10 Release
- 11
- 12 Ext. C.V.
- 13 MOD FR (Dynamics)
- 14 MOD FR
- 15 (Pitch Bend) Dyn.

A - D - Wandler (hardware controlled).

Anin / I/O Board
Faden - Ablesung 360A



A - D.
Tecker-Sockel = 1

7407 = 2

74377 = 3

74374 = 4

4040 = 5

4011 = 6

4001 = 7

LDA A - 0-Port - Data

ORA A # Bit hochsetzen (Reset)

STA A - 0-Port

LDA B - 1-Port - Digitalwert ablesen

STA B - Merken

LDA B # Mux-Adresse (von 0-7)

STA B 0-Port - MUX

AND A # Bit zurücksetzen (Reset)

END

Analog Eingänge:

A, P, D, S, R

Mod. Speed

Mod. Freq

Mod. Delay?

Pitch - Summe

Ext.

GND - Ref.?

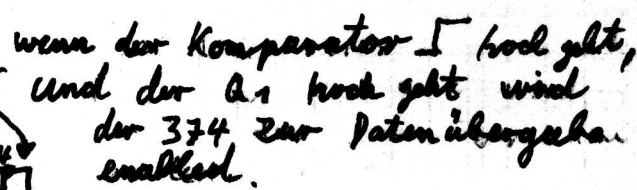
+ - Ref.?

Filter?

"Tact. Latency"

Siehe Bist lassen sich nur ausrechnen, das P. Bit wird für die Begrenzung benötigt.

1/0 Bond
360 KB

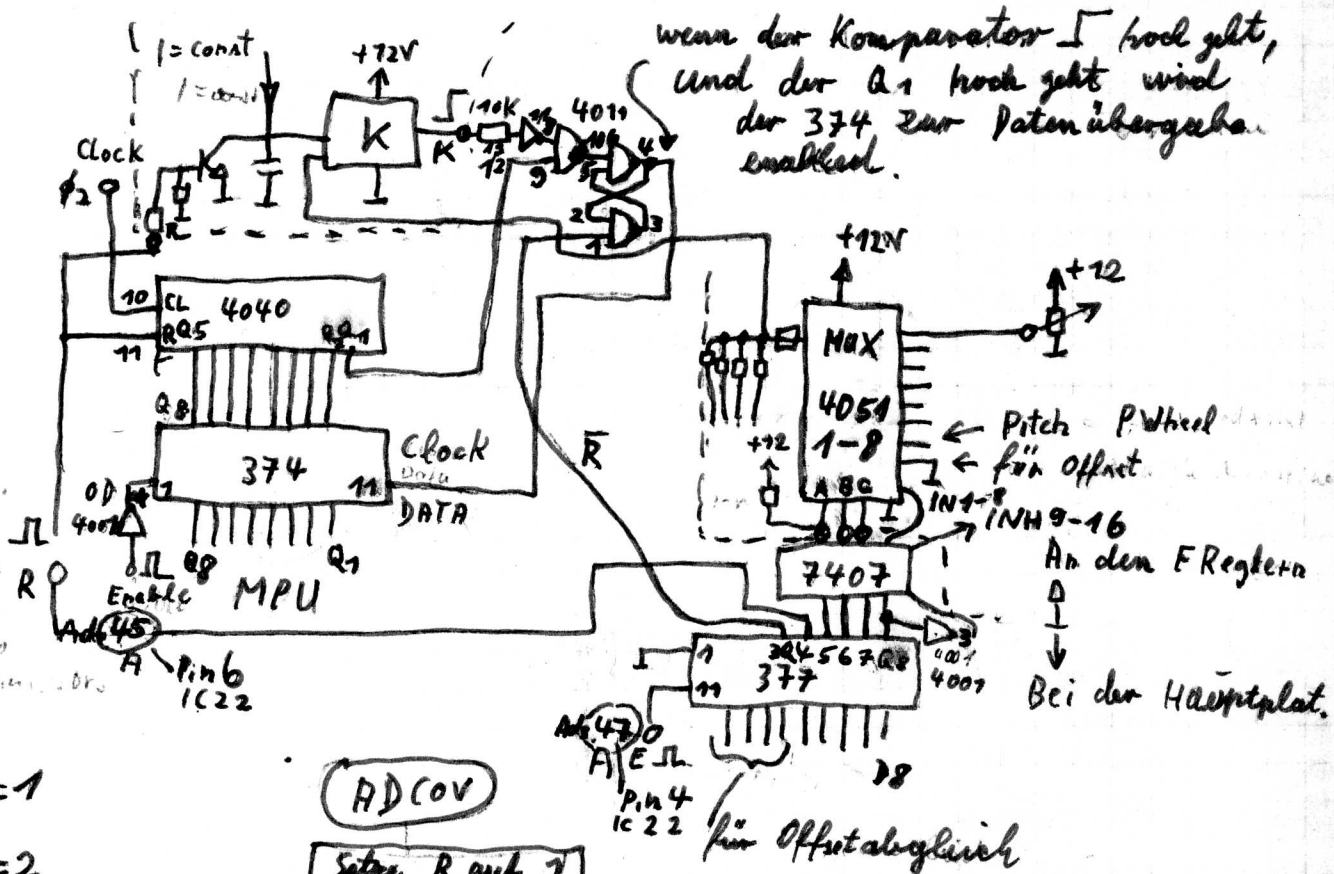


Die sieben Bits lassen sich nur auswerten,
das 8. Bit wird für die Begrenzung benötigt.

Tom. 1000

A-D - wandler (hardware controlled).

I/O Board
360 KB



A.-D.
Stecker-Sockel=1

7407 = 2

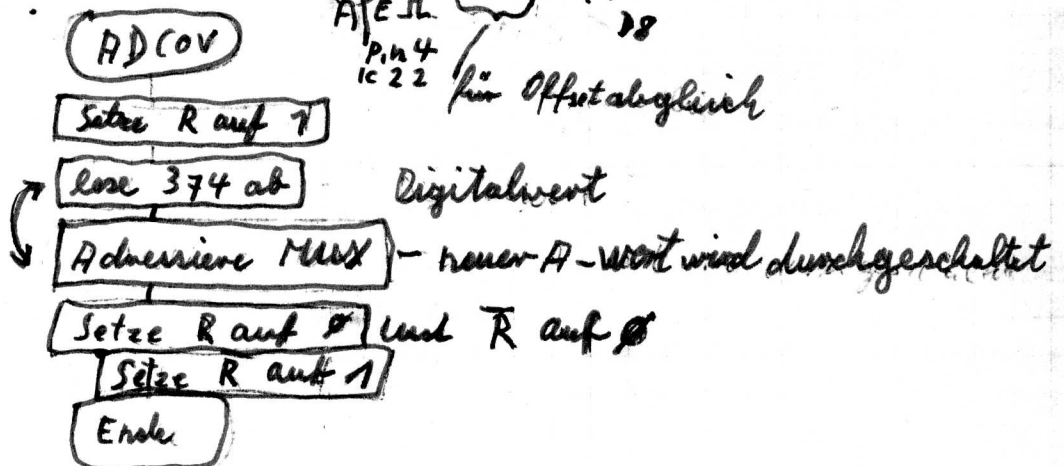
74377 = 3

74374 = 4

4040 = 5

4011 = 6

4001 = 7



```

LDA A - 0-Port-Data
BRA A # Bit hochsetzen (Reset)
STA A - 0-Port
LDA B - 1-Port - Digitalwert ablesen
STA B Speicher
LDA B # MUX-Adresse (von 0-7)
STA B 0 Port MUX
AND A # Bit runtersetzen (Reset)
END

```

Analog Eingänge

Sicher lässt sich nur ausrechnen, dass das 8. Bit wird für die Begrenzung benötigt.

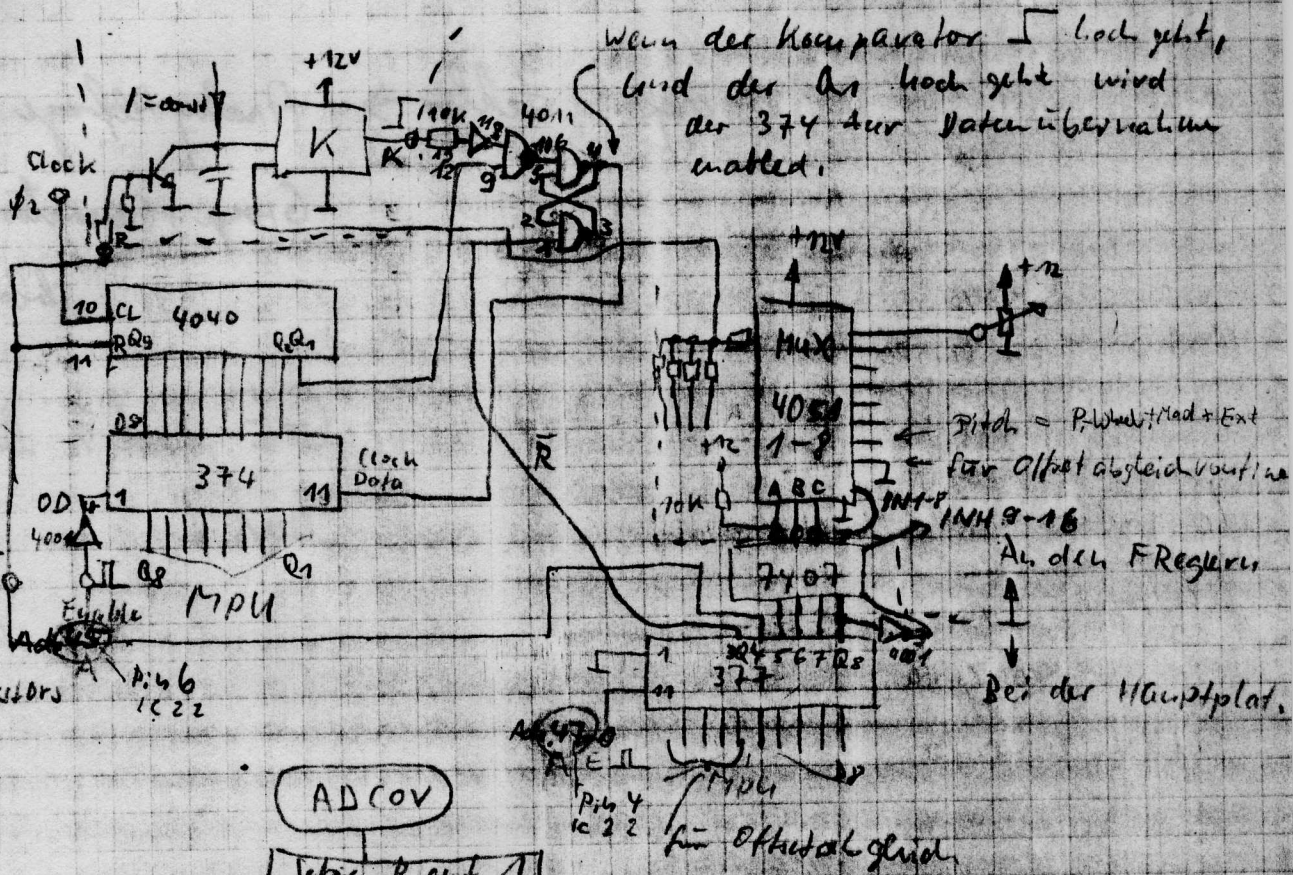
sieben Bits lassen sich nur auswerten, das 8. Bit wird für die Begrenzung benötigt.

GND - Ref. ?
+ Ref.

Transistor

A-D-Wandler (Hardware Controlled).

Anin / 1/0 Board
Faden-Abfrage 360A



A-D.
Tecker-Sockel = 1

7407 = 2

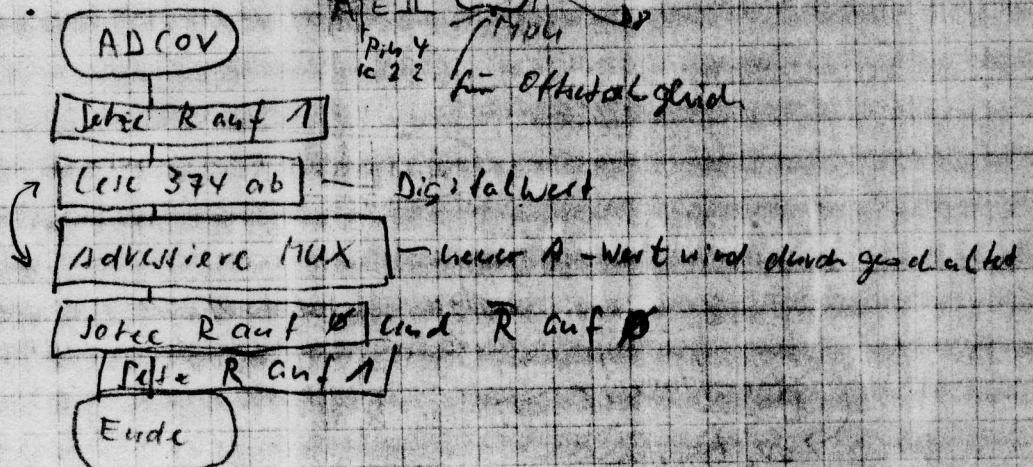
74377 = 3

74374 = 4

4040 = 5

4011 = 6

4001 = 7



```

LDA A - 0-Port-Data
ORA A # Bit hochsetzen (Reset)
STA A - 0-Port
LDA B - 1-Port - Digitalwert ablesen
STA B - Memorie
LDA B # Mux-Adresse (von 0-7)
STA B 0-Port - MUX
AND A # Bit zurücksetzen (Reset)
END
    
```

Analog Ergänzungen:

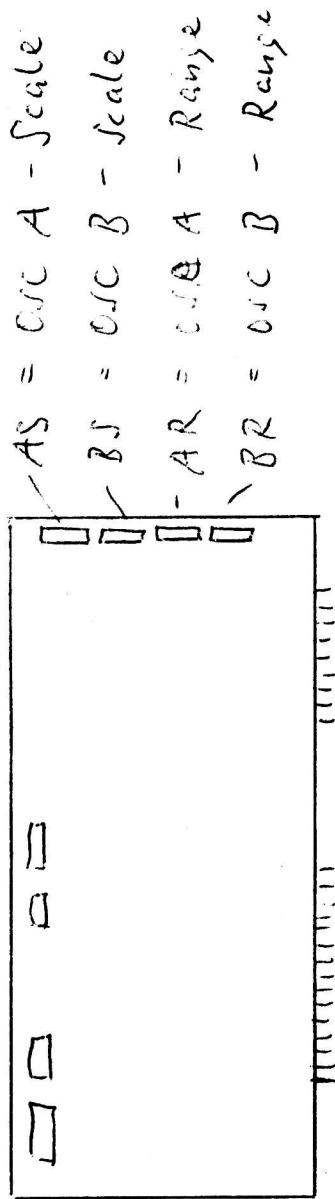
A, P, D, S, R
Mod. Speed
Mod. Freq
Mod. Delay?
Pitch - Summe
Ext.
GND - Ref.?
+ - Ref.?
Filter?
"Tact. Latency"

Siehe B. 5.10 kann sich nur ausrechnen,
das P. Bit wird für die Begrenzung
benötigt.

4077 def: Fehlen $\rightarrow$ Analog Abfrage blockiert
Group + Generator Auswahl
blockiert

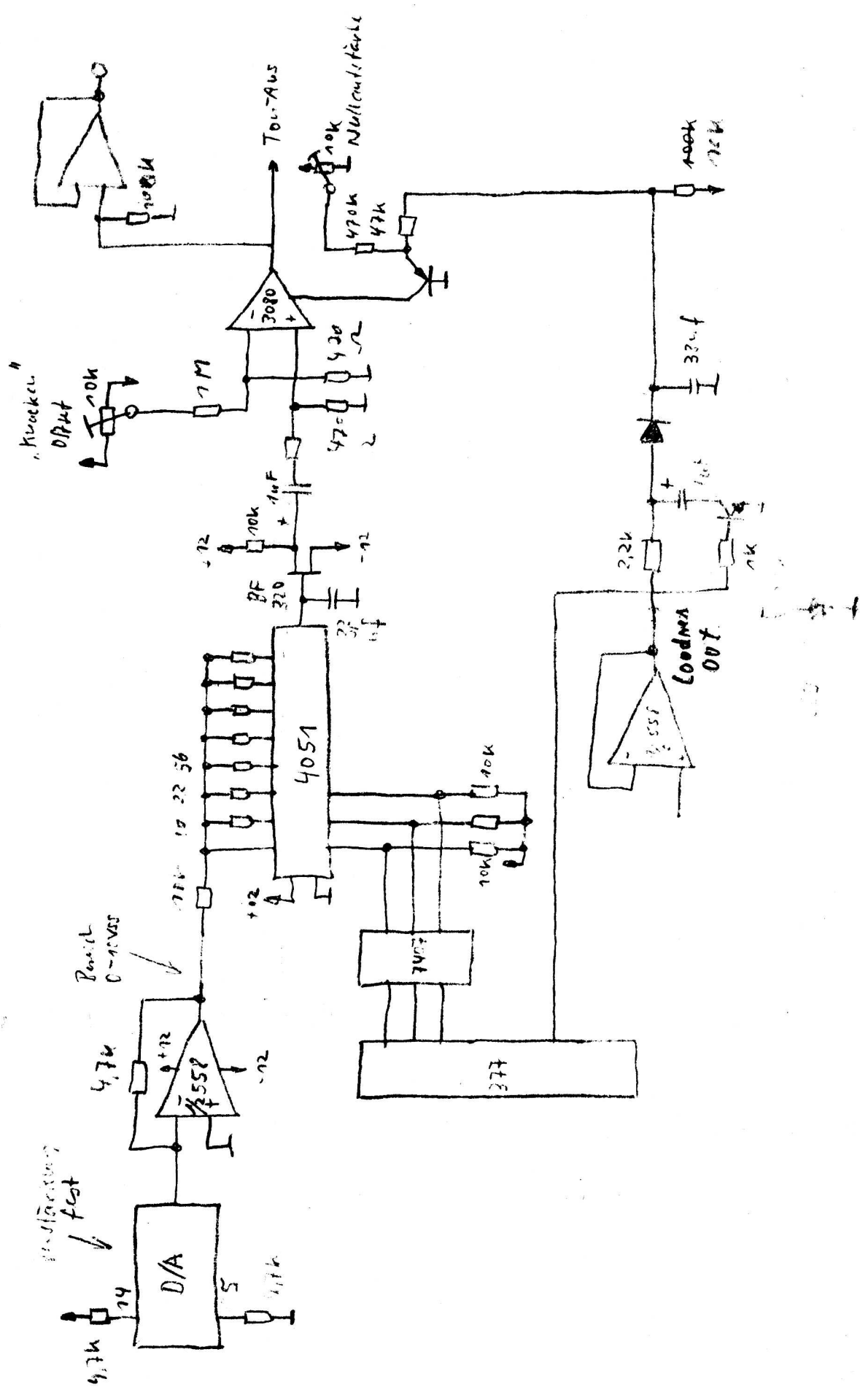
GE Led's bleiben alle
aus!

PPG 260 Oscillator Tuning

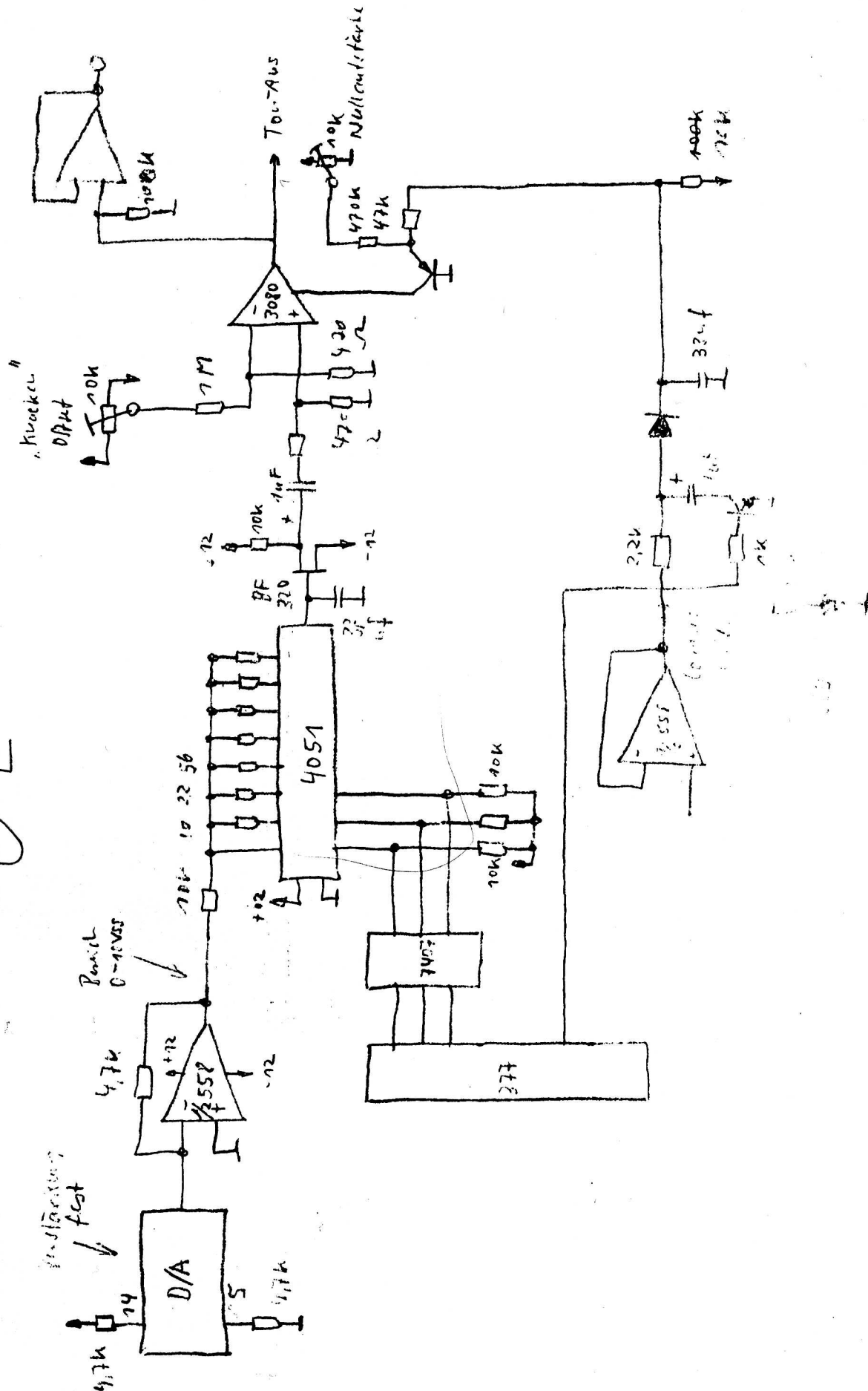


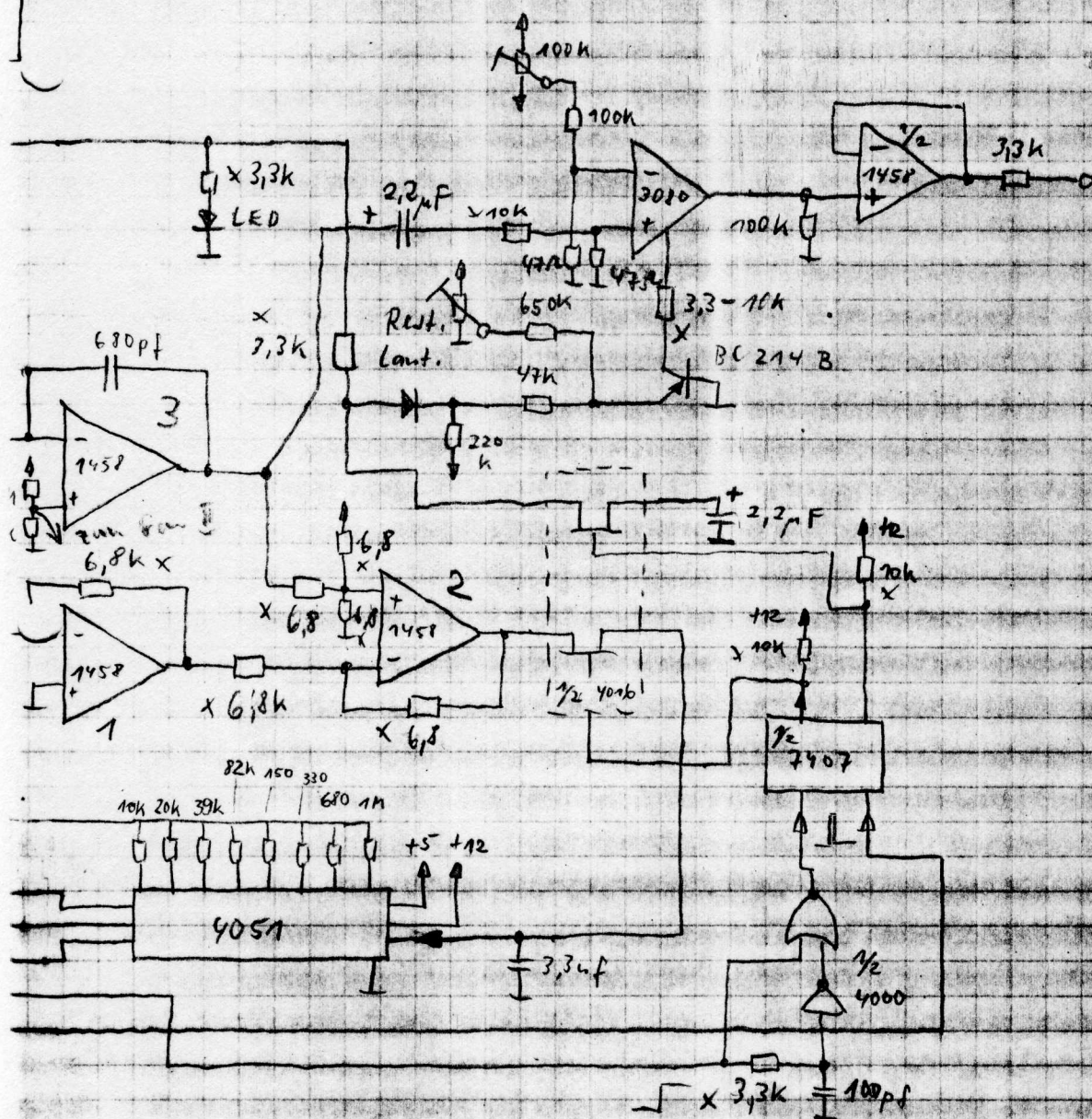
Each of the eight Oscillators have to be tuned as follows:

- 1, Press Note A[#] (B^b) and tune with trim potentiometer "RANGE"
 - 2, Press Note B (H) and tune with trim potentiometer "SCALE"
- repeat this



LD





```

ORG $6100
*** MEMORY TEST
*** WALKING ADDRESS T
EST
  LDAA #$41
  STAA $A017
  JSR OUTCHR
WA22 LDAA $A002
  LDAB $A003
  LDX $A002
WA23 TST $A017
  BEQ WA230
  STAA X
WA230 CMPA X
  BEQ *+5
  JSR ERROR
  CPX $A004
  BEQ WA31
  INX
  TST $A017
  BEQ WA231
  STAB X
WA231 CMPB X
  BEQ WA24
  PSHA
  TBA
  JSR ERROR
  PULA
WA24 CPX $A004
  BEQ WA31
  INX
  ADDB #2
  ADCA #0
  BRA WA23
WA31 TST $A017
  BEQ PAT
  CLR $A017
  BRA WA22
*** PATTERN TESTS
PAT LDAA #$42
  JSR OUTCHR
  LDAA #$FF
  BSR STOREA
  LDAA #$43
  JSR OUTCHR
  LDAA #$AA
  BSR STOREA
  LDAA #$44
  JSR OUTCHR
  LDAA #$55
  BSR STOREA
  LDAA #$45
  JSR OUTCHR
  CLRA
  BSR STOREA
  BRA WBTST
STOREA LDX $A002
  DEX
ST31 INX
  STAA X
  CPX $A004
  BNE ST31
  LDX $A002
  DEX

```

auf Cassette

```

ST42 INX
  CMPA X
  BEQ *+5
  JSR ERROR
  CPX $A004
  BNE ST42
  RTS
WBTST LDAA #$57
  JSR OUTCHR
  LDX $A002
  BRA WB00
WBNWAD LDX $A017
  CPX $A004
  BNE WB0
  JMP REENTR
WB0 CLR X
  INX
WB00 STX $A017
  LDAB #10000000
  BRA WB1
WBNWBT LSRB
  BCS WBNWAD
WB1 LDX $A017
  STAB X
  LDX $A002
  BRA WB2
WBCKME CPX $A004
  BEQ WBNWBT
  INX
WB2 CPX $A017
  BEQ WBBT
  LDAA X
  BEQ WBCKME
  CLRA
WBERR BSR ERROR
  BRA WBCKME
WBBT TBA
  CMPB X
  BNE WBERR
  BRA WBCKME
ERROR PSHA
  STX $A013
  STAA $A015
  LDAA X
  STAA $A016
  LDX #MCL
  JSR PDATA1
  LDX #$A013
  JSR OUT4HS
  JSR OUT2HS
  JSR OUT2H
  PULA
  LDX $A013
  RTS
MCL FCB $A,$D,$14,$0,$0,
0,$0,$2A,$4
  END

```


Auf 2708 EPROM

```

NAM PROM-PROGRAMMER (2
708)
OPT M.O.NOP.S
ORG $6000
OUT2H EQU $FD76
OUTCHR EQU $FD0B
PDATA1 EQU $FD33
OUT2HS EQU $FD81
OUT4HS EQU $FD7F
REENTR EQU $FC43
PIAA EQU $B100    DATE
NSTEuerung
PIAB EQU $B102    ADRE
SSTeuerung
OPOR EQU $B801    A8.A
9.CONTROL

```

```

LDS #$7F
CLRA
STAA PIAB+1
LDAB #$FF
STAB PIAB
STAA PIAA+1
STAB PIAA
LDAA #4
STAA PIAA+1
STAA PIAB+1

```

```

CLRA
ORAA #4
STAA OPOR
LDX #$12C
STX $14
P1 LDX 4
STX $10
LDX 0
STX $12
P2 LDX $12
LDAA X
STAA PIAA
LDAA $11
STAA PIAB
LDAA $10
ANDR #3
ORAA #4
STAA OPOR
ANDR #3
INX
STX $12
STAA OPOR
LDX #$32
Z1 DEX
BNE Z1
ORAA #4
STAA OPOR
LDX $10
CPX 2
BEQ P3
INX
STX $10
BRA P2

```

```

P3 LDX $14
DEX
BEQ P4
STX $14
BRA P1
P4 LDX $FFFF
Z2 DEX
BNE Z2
LDX 0
STX $12
LDX #0
STX $16
LDX 4
STX $10
LDAA #$C
STAA OPOR
CLRA
STAA PIAA+1
STAA PIAA
LDAA #4
STAA PIAA+1
LDX $FFFF
Z3 DEX
BNE Z3
P5 LDAA $10
ANDR #3
ORAA #$C
STAA OPOR
LDAA $11
STAA PIAB
LDAA PIAA
LDX $12
CMPA X
BNE P7
P6 INX
STX $12
LDX $10
CPX 2
BEQ P8
INX
STX $10
BRA P5
P7 STAA $20
LDAA X
STAA $21
LDX $10
STX $22
LDX #$20
JSR OUT2HS
JSR OUT2HS
JSR OUT4HS
LDX $16
INX
STX $16
LDX $12
BRA P6
P8 LDX #$16
JSR OUT2HS
JSR OUT2HS
JMP REENTR

```

Testprogramm für A-D-Converter (16 Kanäle)

Die 16 Analogwerte werden auf dem Monitor als Zeichen sichtbar.

Abbildung der Analogplätze:

FR ganz unten → L Alpha

FR ganz oben → □ Space

```
NAM ANIN *TEST
OPT M.NOP.0.5
ORG $9000
MUX EQU $A003 *SELECT
MERK.
AX EQU $C010 *RAM
MX EQU $A004 *X-MERKER
```

```
LDS #$A07F
AN1 JSR ANIN
LDX #$20
Z DEX
BNE Z
BRA AN1
*****
ANIN LDAA MUX
ORAA #%00001000 *RESE
T
STAR $B047
LDX MX
INX
ADDA #$10 *NEU SELECT
```

```
BCC AN2
LDX #AX
***AUSWERTUNG
***FENSTER(00-7F)
AN2 STX MX
LDAB $B045 *ANALOG DA
TA
BMI AU1
SUBB #$0C
BPL AU2
CLRB
AU2 STAB X
ANDR #%11110011 *RES
AUS.FL-FL TRIG
STAR $B047
ORAA #%00000100 *FL-F
L TRIG AUS
STAR MUX
STAR $B047
RTS
AU1 SUBB #$0C
BPL AU2
LDAB #$7F
BRA AU2
END
```

Unterprogramm:

"ANIN"

Testprogramm

für Memory 0080 - 00FF
G 6120

für Memory 0200 - 03FF
G 6122

für I-O - Enable, wobei die
Adresse hier eingegeben werden
kann

G 6124

```
NAM TEST
OPT M.O.NOP.S
ORG $9000
BRA MEM1
BRA MEM2
BRA ENAB
BRA INOT
LDS #$A07F
MEM1 LDX #$80
STX $A002
LDX #$FF
STX $A004
JSR $E180
JSR $E2F1
MEM2 LDX #$200
STX $A002
LDX #$3FF
STX $A004
JSR $E180
JSR $E2F1
ENAB LDX #TAB ← ist
JSR $E130      Text
JSR $E0D9      relativ
CLRB
T2 INC $A002
BNE T3
SEC
ROL $A003
BPL T3
CLR $A003
INCB
T3 STAB X
LDAA $8009
CMPA #$1B = ESC
BNE T4
JMP $E040
T4 CMPA #$0D = CR
BNE T2
BRA ENAB
BRA T2
INOT SWI
TAB FCB $0A
FCB $0D
FCB $41
FCB $44
FCB $52
FCB $45
FCB $53
FCB $53
FCB $45
FCB $3E
FCB $04
END
```

Event Buffer Transfer

Test

Text " <↑> ADRESSE "

Testprogramm

für Memory 0080 - 00FF
G 6120

```
NAM TEST
OPT M.O.NOP.S
ORG $9000
BRA MEM1
BRA MEM2
BRA ENAB
BRA INOT
LDS #$A07F
MEM1 LDX #$80
STX $A002
LDX $FF
STX $A004
JSR $E180
JSR $E2F1
MEM2 LDX #$200
STX $A002
LDX $3FF
STX $A004
JSR $E180
JSR $E2F1
ENAB LDX #TAB ← ist
JSR $E180      nicht
JSR $E0D9      aktiv
CLRB
T2 INC $A002
BNE T3
SEC
ROL $A003
BPL T3
CLR $A003
INCB
T3 STAB X
LDAA $8009
CMPA #$1B = ESC
BNE T4
JMP $E040
T4 CMPA #$0D = CR
BNE T2
BRA ENAB
BRA T2
INOT SWI
TAB FCB $0A
FCB $0D
FCB $41
FCB $44
FCB $52
FCB $45
FCB $53
FCB $53
FCB $45
FCB $3E
FCB $04
END
```

für Memory 0200 - 03FF
G 6122

für I-O - Enable, wobei die
Adresse hier eingegeben werden
kann
G 6124

Event Buffer Transfer
Test

} Text " <↑> ADRESSE "

```

NAM MONITOR
OPT M.O.NOP
ORG $9000
LDX #A07F
STX A008
LDX #E227
STX A00A
LDAA #3
STAA $8008
LDAA #11
STAA A019
LDS A008
LDAA A019
STAA $8008
CLR A00C
CLR A049
x ***PIA INIT
LDAA #FF
STAA $B400
LDAA #4
STAA $B401
LDAB #X10000011
STAB $B402
STAA $B403
LDAA #1
STAA $B402
*****
M4 LDAA #00
JSR $E108
LDAA #0A
JSR $E108
LDAA #3E
JSR $E108
JSR $E180
M1 JSR $E115
CMPA #4F
BEQ 01
CMPA #42
BEQ B1
CMPA #44
BEQ D1
CMPA #45
BEQ E1
CMPA #39
BEQ G1
CMPA #20
BNE M1
JMP $E040
01 JSR $E108
JMP $6124
B1 LDAB #81
STAB $B402
JSR $E108
JMP $644F
E1 LDAB #81
STAB $B402
JSR $E108
JMP $7915
G1 JSR $E108
JMP $9000
D1 LDAB #81
STAB $B402
JSR $E108

```

```

ASZ EQU A070 UND 1
HSP1 EQU A072
HSP2 EQU A073
HSP3 EQU A074
ZAH1 EQU A075
Z1 EQU A076
HSPX EQU A077 UND 8
HSP4 EQU A079
ZZPROZ EQU 22
ANFCOD EQU $D6B0
LDX #01FE
STX ASZ
CLR HSP1
CLR HSP3
LDAA #2
STAA HSP2
LDAA #ZZPROZ
STAA ZAH1
H2 LDAA $B402
BITA #10
BNE H2
HAUPT BSR STAM
LDAA #5
STAA HSP4
H1 BSR GLEER
DEC HSP4
BNE H1
HAUPT1 BSR HOASC
CMPA #D
BEQ HAUPT2
CMPA #FF
BEQ HAUPT3
BSR EACT
BSR GZAUSH
DEC ZAH1
BNE HAUPT1
HAUPT2 LDAA #ZZPROZ
STAA ZAH1
BSR WZEND
BRA HAUPT1
HAUPT3 BSR GLEER
BSR STOM
HAUPT4 LDAA $B402
BITA #10
BNE HAUPT4
BSR STAM
BSR GLEER
BSR STOM
BRA HAUPT4
GLEER LDAA $B402
BITA #4
BNE GLEER
BSR WZEND
RTS

```

```

WZEND LDAA $B402
TAB
COMA
ANDA HSP3
STAB HSP3
BITA #4
BEQ WZEND
LDAB #80
D0 DEC8
BNE D0
LDAA $B402
BITA #4
BNE WZEND
CLR HSP3
RTS
STAM LDAA $B402
ORAA #2
STAA $B402
RTS
STOM LDAA $B402
ANDA #FD
STAA $B402
RTS
GZAUSH BRA GZAUS
HOASC LDX ASZ
LDAA 0,X
INX
STX ASZ
RTS
EACT LDX #ANFCOD
STX HSPX
SUBA #20
TAB
ASLA
ASLA
ABA
BCC EACT1
INC HSPX
EACT1 ADDA HSPX+1
BCC EACT2
INC HSPX
EACT2 STAA HSPX+1
LDX HSPX
RTS
GZAUS LDAA #5
STAA Z1
GZAUS1 LDX HSPX
LDAA 0,X
INX
STX HSPX
BSR AUSSP
DEC Z1
BNE GZAUS1
CLRA
BSR AUSSP
CLRA
BSR AUSSP
RTS

```

NAM DRUCKER
 OPT M.O.NOP
 ORG \$9000
 ASZ EQU \$A070 UND 1
 HSP1 EQU \$A072
 HSP2 EQU \$A073
 HSP3 EQU \$A074
 ZAHL EQU \$A075
 Z1 EQU \$A076
 HSPX EQU \$A077 UND 8
 HSP4 EQU \$A079
 ZZPROZ EQU 22
 ANFCOD EQU \$D523
 STACKP EQU \$A07F
 LDS #STACKP
 LDX #\$01FE
 STX ASZ
 CLR HSP1
 CLR HSP3
 LDAA #2
 STAA HSP2
 LDAA #ZZPROZ
 STAA ZAHL
 LDAA #\$FF
 STAA \$B400
 LDAA #4
 STAA \$B401
 LDAA #3
 STAA \$B402
 LDAA #4
 STAA \$B403
 H2 LDAA \$B402
 BITA #\$10
 BNE H2
 HAUPT BSR STAM
 LDAA #5
 STAA HSP4
 H1 BSR GLEER
 DEC HSP4
 BNE H1
 HAUPT1 BSR HORASC
 CMPA #\$D
 BEQ HAUPT2
 CMPA #\$FF
 BEQ HAUPT3
 BSR EACT
 BSR GZAUSH
 DEC ZAHL
 BNE HAUPT1
 HAUPT2 LDAA #ZZPROZ
 STAA ZAHL
 BSR WZEND
 BRA HAUPT1
 HAUPT3 BSR GLEER
 BSR STOM
 HAUPT4 LDAA \$B402
 BITA #\$10
 BNE HAUPT4
 BSR STAM
 BSR GLEER
 BSR STOM
 BRA HAUPT4

GLEER LDAA \$B402
 BITA #4
 BNE GLEER
 BSR WZEND
 RTS
 WZEND LDAA \$B402
 TAB
 COMA
 ANDA HSP3
 STAB HSP3
 BITA #4
 BEQ WZEND
 LDAB #\$80
 D0 DECB
 BNE D0
 LDAA \$B402
 BITA #4
 BNE WZEND
 CLR HSP3
 RTS
 STAM LDAA \$B402
 ORAA #2
 STAA \$B402
 RTS
 STOM LDAA \$B402
 ANDA #\$FD
 STAA \$B402
 RTS
 GZAUSH BRA GZAUS
 HORASC LDX ASZ
 LDAA 0.X
 INX
 STX ASZ
 RTS
 EACT LDX #ANFCOD
 STX HSPX
 SUBA #\$20
 TAB
 ASLA
 ASLA
 ABA
 BCC EACT1
 INC HSPX
 EACT1 ADDA HSPX+1
 BCC EACT2
 INC HSPX
 EACT2 STAA HSPX+1
 LDX HSPX
 RTS
 GZAUS LDAA #5
 STAA Z1
 GZAUS1 LDX HSPX
 LDAA 0.X
 INX
 STX HSPX
 BSR AUSSP
 DEC Z1
 BNE GZAUS1
 CLRA
 BSR AUSSP
 CLRA
 BSR AUSSP
 RTS

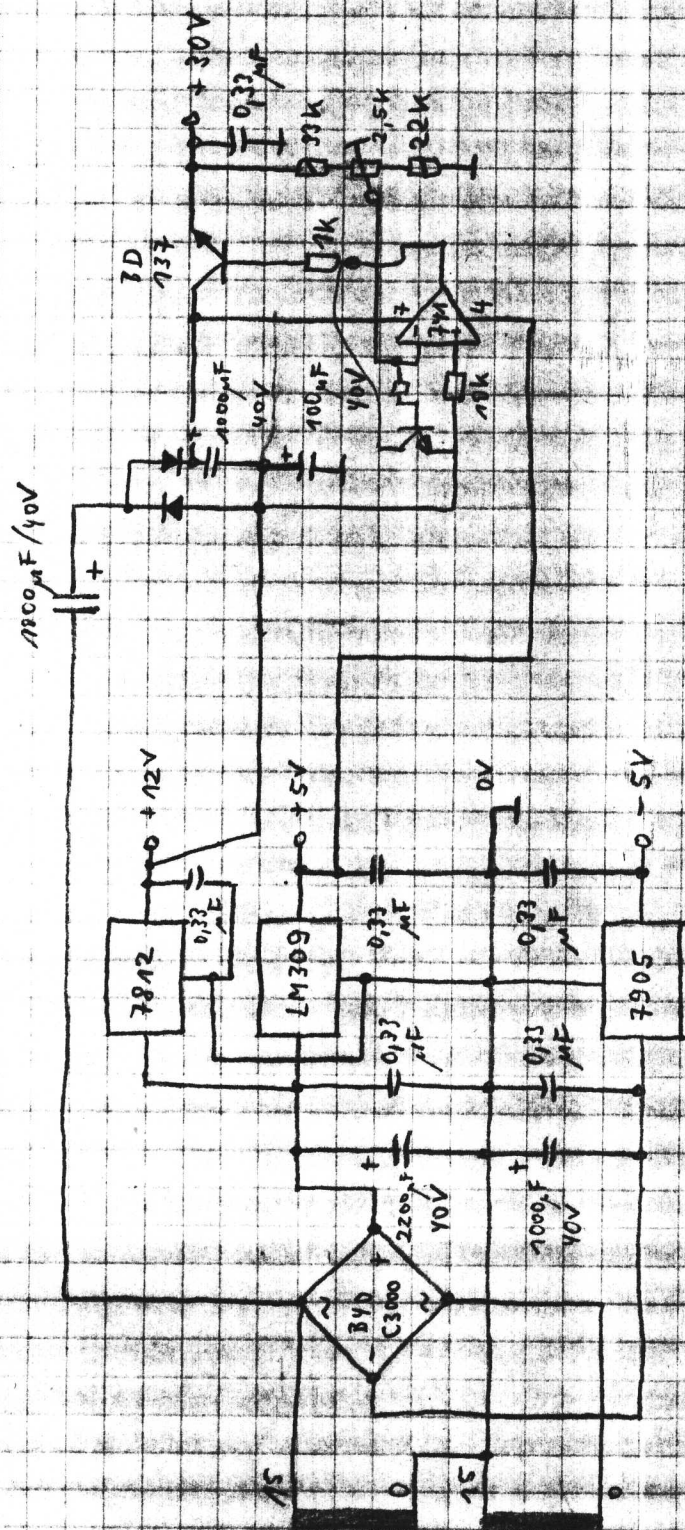
AUSSP STAA \$B400
 AUSSP1 LDAA \$B402
 TAB
 ANDA HSP1
 COMB
 STAB HSP1
 BITA #8
 BNE AUSSP1
 DEC HSP2
 BNE AUSSP1
 LDAB #30
 STAB HSP2
 LDAA \$B402
 ANDA #\$FE
 STAA \$B402
 LDAB #\$80
 AUSSP2 DECB
 BNE AUSSP2
 ORAA #1
 STAA \$B402
 RTS
 END

Handwritten notes:
 } 2500000
 Pals

2



Hand-drawn circuit diagram of a precision rectifier using two op-amp ICs (7812, LM309, 7905) and various passive components. The circuit includes a 30V supply, a 1000µF/40V capacitor, and a 7812 regulator. The LM309 is configured as a precision rectifier with a 2200µF/40V capacitor and a 1000µF/40V capacitor. The 7905 is configured as a negative voltage regulator with a 0.33µF capacitor. The output is labeled 0V and -5V.



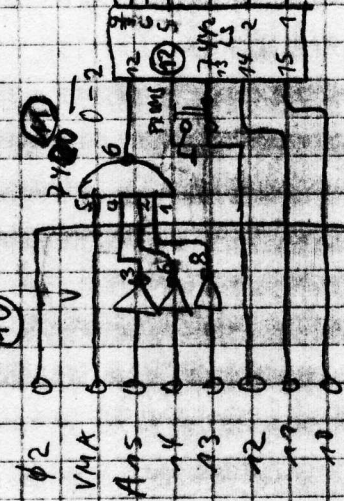
Digitaler Einsabeplatte „Poly“

Beschreibung		I-Port, Bit		LED - O-Port, Bit	
Taster	Progr. No., KB	88	B006	—	
Taster	Keyboard Mode Step	80	B006	—	
"	Update OFF, A, B, C	01	B006	B003	, 1
"	Parameter No., KB	88	B006	B005	, 1
"	Magnitude Step 5	80	"	B005	, 2
"	TUNE 0-7	01	"	B003	, 2
"	SEMITONE, 0-9	01	"	B003	, 3
"	Key Balance 0-7	80	"	B003	, 8
"	Envelope Mode 0-2	80	"	—	
"	Keyb. Dyn. Rcting. 0-3	80	"	—	
Ziffernanszeige Keyb. Mode		—		B001	Byte 10-19
Parameter / Progr. No.		—		B001	Byte 20-29, 30-39
Voice No.		—		B001	Byte 40-49

Taster "0" - "9" - Extra Keyb	08	B006
Taster "X, XX" ...	10	B006
	20	B006
= max. 32 Tasten	40	B006

Poly RAM / ROM Interface

74LS00

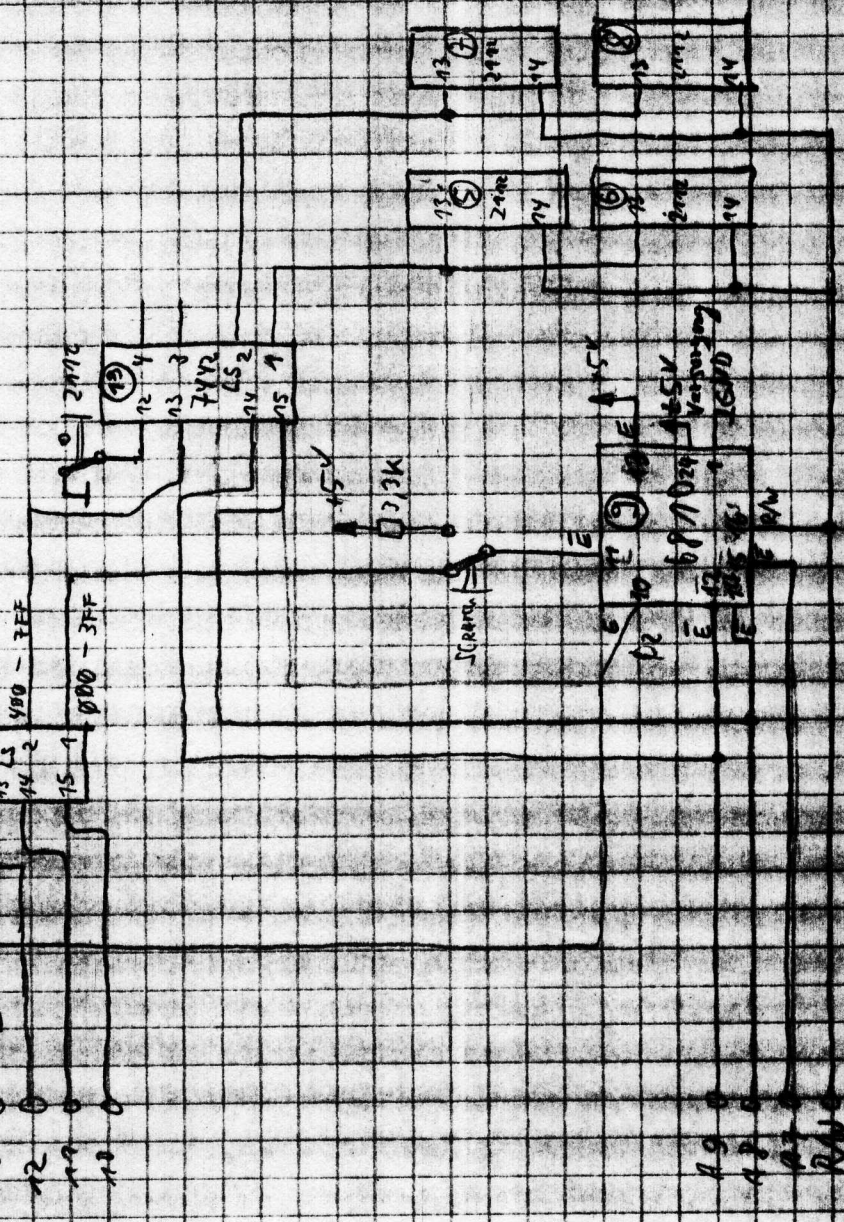


1C00 - 1FF → 1C0
1A00 - 1BF → 1C0
1B00 - 13FF → 1C0
1C00 - 13FF → 1C0

Pin 1800 GND

Ans	14	12	10	8	6	4	2
0	1	0	1	0	1	0	1

Alt



1000 - 05FF
6810 - 0000 - 00FF
1000 - 00FF

A

1000

19 0
18 0
17 0
16 0

15 24
GND

Poly RAM / ROM Interface

Alt

74LS00

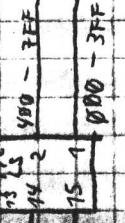


- Pin 1
- Pin 2
- Pin 3
- Pin 4
- Pin 5
- Pin 6
- Pin 7
- Pin 8
- Pin 9
- Pin 10
- Pin 11
- Pin 12
- Pin 13
- Pin 14
- Pin 15
- Pin 16

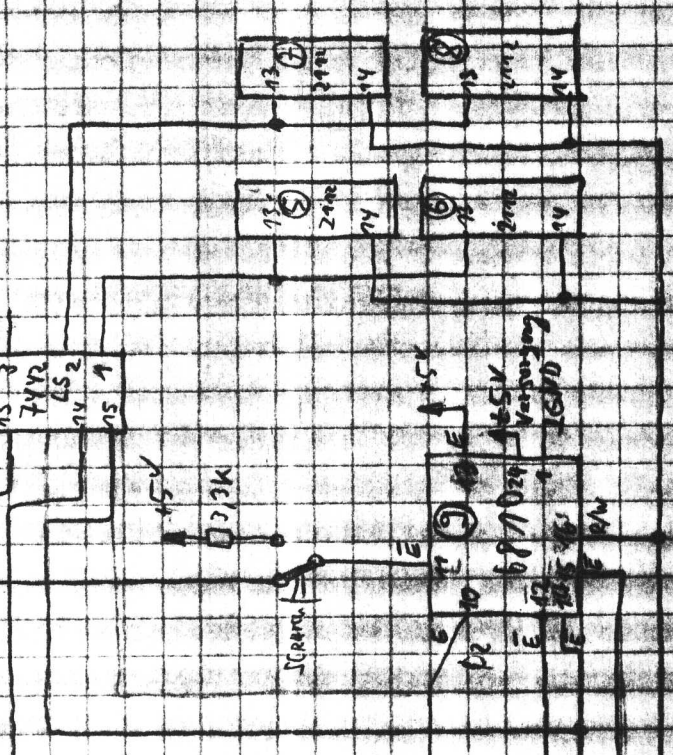
1200 - 1FFF → 1C0
1800 - 1BFF → 1C5
1900 - 13FF → 1C0
1000 - 13FF → 1C0

Pin 1800 GND

Pin 1800 GND



- Pin 1
- Pin 2
- Pin 3
- Pin 4
- Pin 5
- Pin 6
- Pin 7
- Pin 8
- Pin 9
- Pin 10
- Pin 11
- Pin 12
- Pin 13
- Pin 14
- Pin 15
- Pin 16



2100 - 05FF
6810 - 0000 - 00FF
1000 - 1FFF

A

10000

15 24
GND

Änderung RAM

1/2. Reihe R/W aufnehmen (5101 zum 2114)

2, am 74 CS 04 unten mit, Massebahn →

Punkt abtrennen

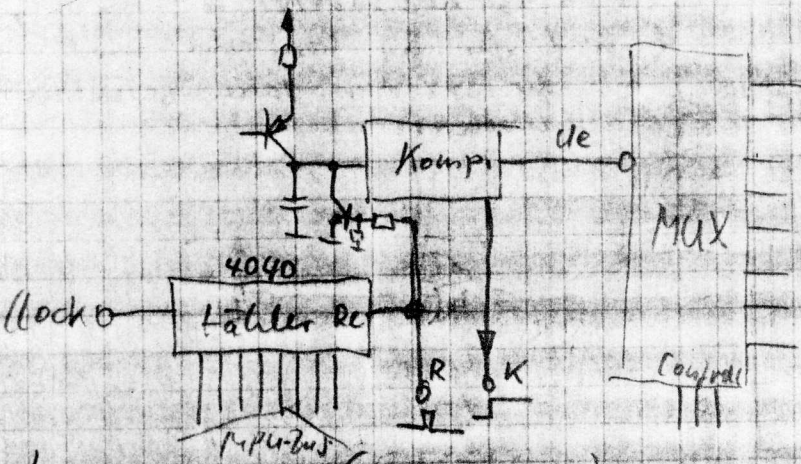
3, an 5101 oben ~~mit~~ "F"

Rückseite Bahn von "Pis 18 (4. v. oben)

nach 19 (3. v. oben) umlegen

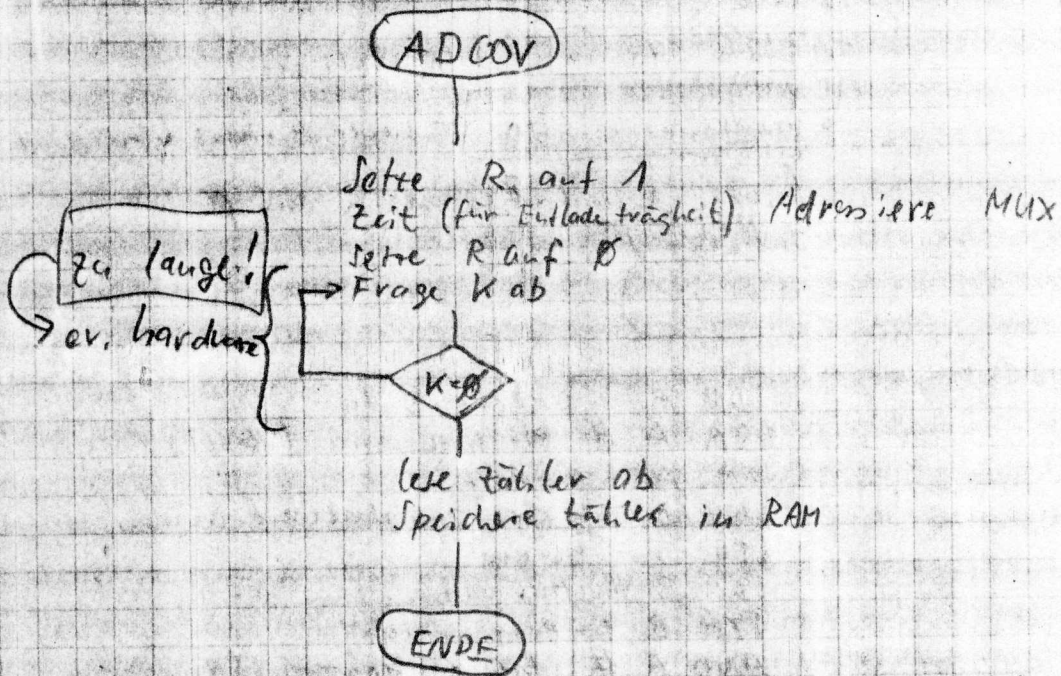
KM 60. → August.

A-D-Wandler (MPU controlled)



IC suchen mit (Markt + Technik)

- Komparator,
- Countdown-Strategie
- Entlade Transistor



340 / 380 Extra Variable
Pitch wheel

Stecker Anschl.:

Pin 2 = GND

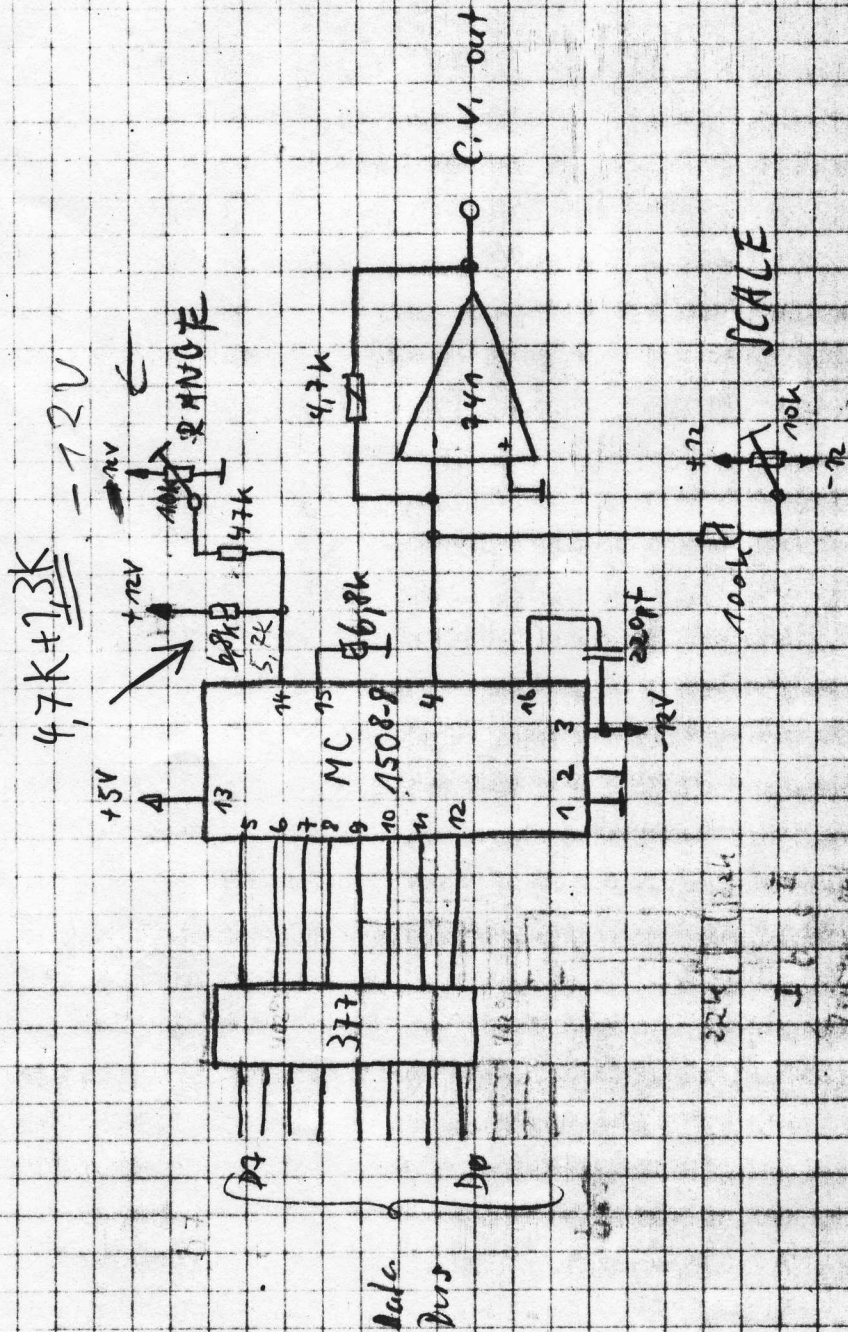
13 = + 12V

5 = Filter/Gene

6 = Pitch wheel

(4 = Op Amp output)

Outputs for Reg. Computer Poly Output D/A



340 - Keyboard Verlabelung

im Einschub (gekotet!)

im Keyboard

Flachkabel → 24 Pol-Buchse

24 Pol-Stecker → Flachkabel

16	→	8
1		7
15		6
2		5
14		4
3		3
13		2
4		1
12		14
5		9
11		10
6		11
10		12
7		13
8		15
		16

1	rt	8
2	bl	7
3	li	6
4	gt	5
5	gn	4
6	ge	3
7	sw	2
8	ts	1
9	bt	14
10	ws	9
11	gt/ts	10
12	ws/ts	11
13	bt/ts	12
14	bl/rt	13
15	bt/gt	15
16	ws/rt	16

16
1
15
2
14
3
13
4
12
5
11
6
10
7
8

bl/bt 17 } Keyb. DMS
ge/bt 18

ge/ws 19 } Pitch oben
ws/gt 20 } Schleifer
bt/rt 21 } Wheel unten

gn/ws 22-24 } frei
bl/ws 23
gn/bt 24

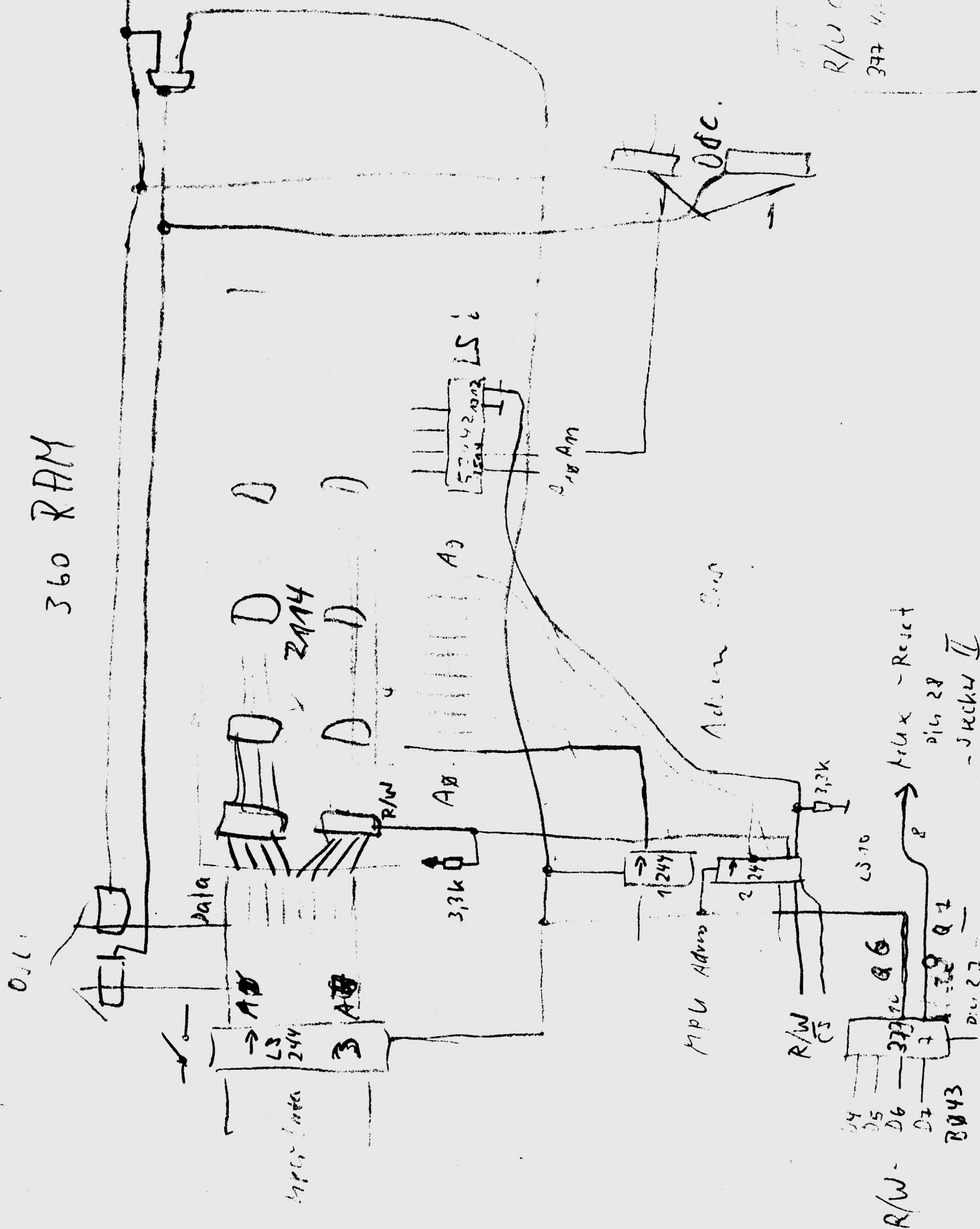
4N1N 21000

2 Extra hoch

1. 1x 1000000 von "freq." $\rightarrow$ 2. 4057 1002

2. 5101 1004 $\rightarrow$ 5101 1004

377 117. 16 24 1 1/2, 11



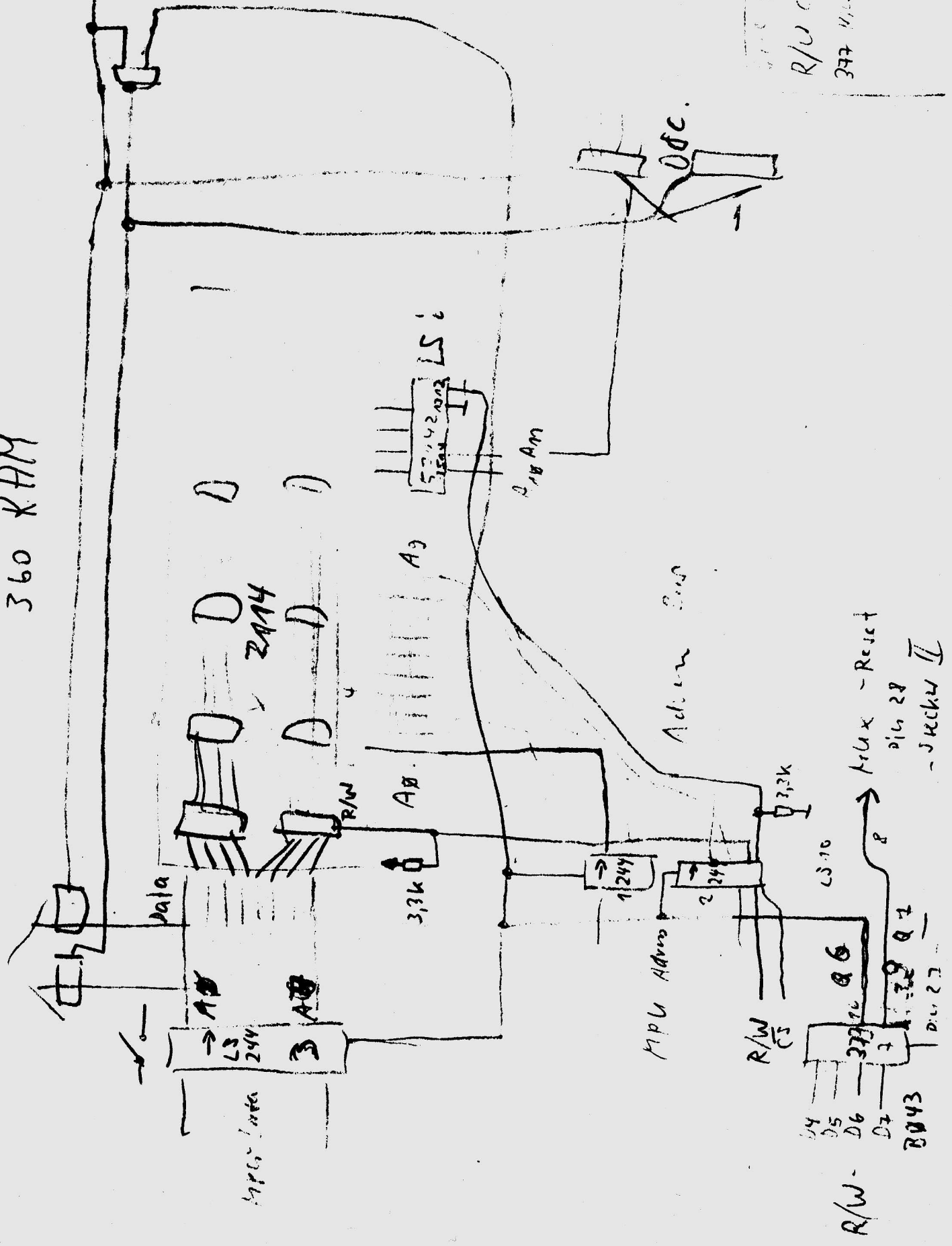
360 RDM

五

10/10/10

R/W on Trimm Co 2014

372 44. 16 24 1 1/2 1



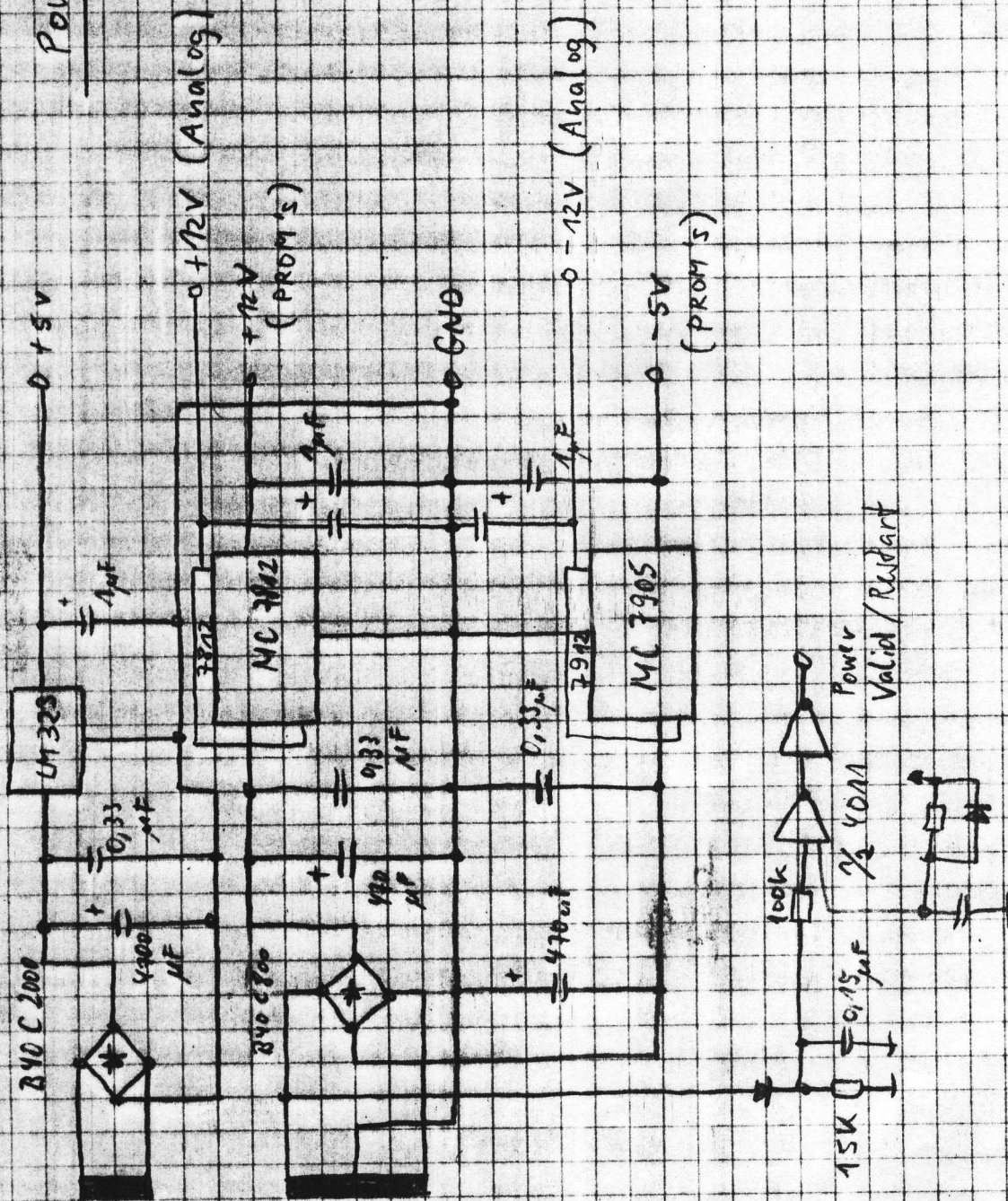
lala



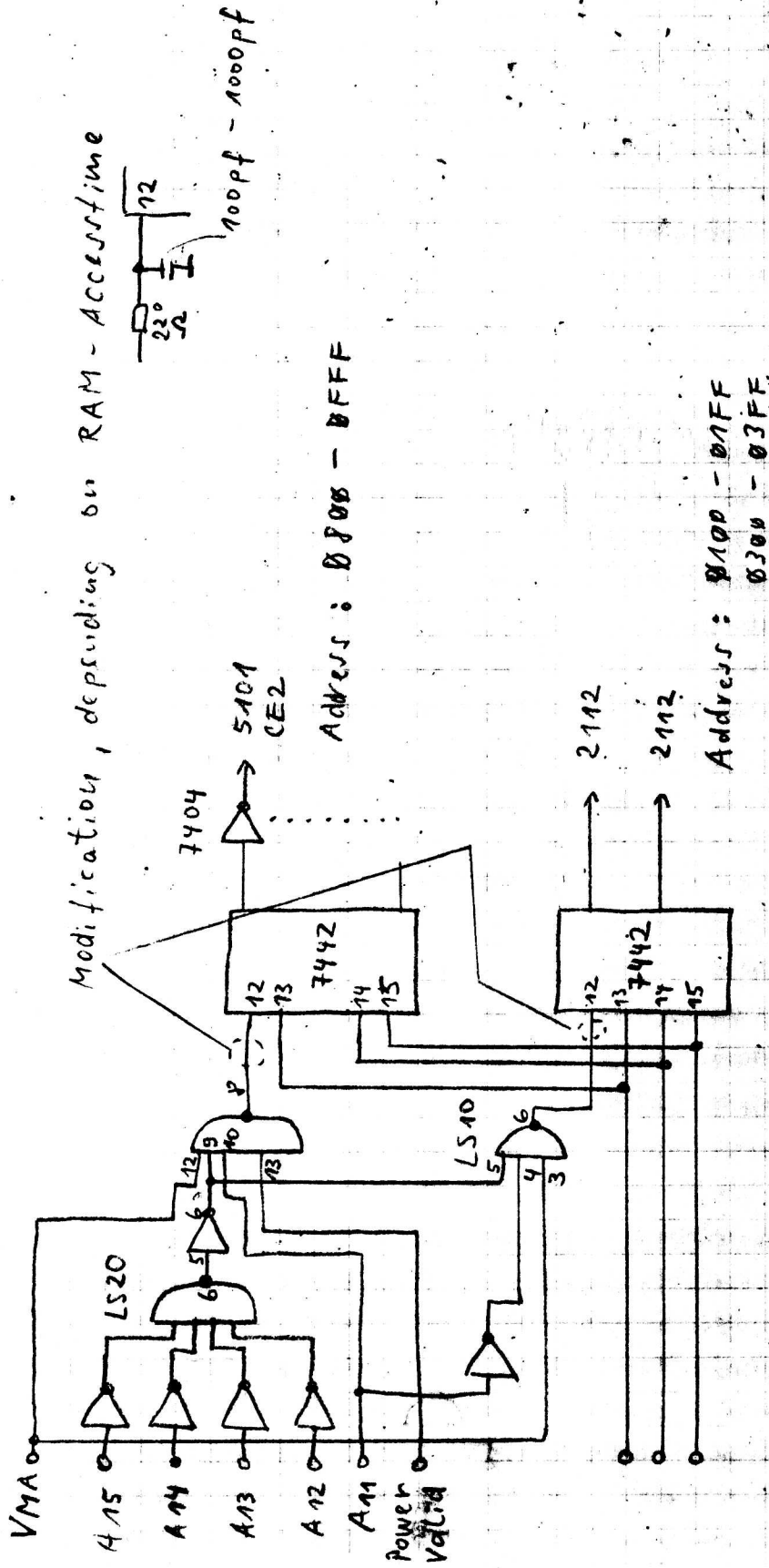
Propr. 11 Taste 29

oder 742 direkt am GND
bei 1000er MAX!

Power Supply 360A



RAM Board 360A



I-O - Poly

B000 }
1
2
3
4
5
6
7 } Digital - Port

B010 -
11 - Keyb. → schreiben ✓
12 - Keyb. ← lesen ✓
13 - Ext. Digital - schreiben ✓
14
15 - Ext. Digital - lesen ✓

B020 -
1
2
3
4
5
6
7 } OSC.
PWN

B030 -
1
2
3
4
5
6
7 } OSC.
Data

B040 - Filter Data - lesen } → Tr: per Input = b1, Filter Flag = b0
1 - D/A Converter
2 -
3 - PWN, (R/W - rate) ✓
4 -
5 - A/D - Output - Data -
6 -
7 - A/D - Select (mux) ✓ + Trig - (300)

B050 - Timer setzen → ACIA (B056, 57)

B060 -
B062 } osc. Filter Data
64
66

B070 = CV. output (D-A-Converter - 12 bits)

Fig 1-0 16 pol Stecker

1 = bp
2
3
4
5
6
7
8 = bz

} MPu Data

9 - A0
10 - A1
11 - A2
12 - R/W
13 - BPPX
14 - GND
15 - 02
16 - +5V

Keyboard Stecker 16 Pol

1
2
3
4
5
6
7
8

} Data - Kontakte

9 - 2.
10 - 3.
11 - 4.
12 - 5.
13 - 6.
14 - unter 1.
15 - 7.
16 - 8.

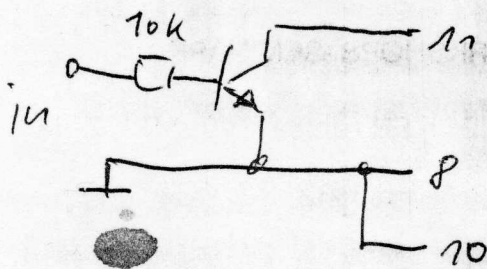
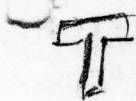
} Sammelrohre

360

Adapter kabel für

V-Trigger über

Bsp. 1-0 input



Pin 1, 2, 3, 6, 7 an GND
Pin 4, 5 offen

Rückseite Buchsen

Mono / Ch 1 → MB
 Ch 2 → MB
 Headphones → MB

Sustain SW → I/O Port 1 Pin 29
 CV in → " Pin 23 → Anin Pin 5
 Gate in → " Pin 30
 Gate out → " Pin 28

Cassette I/O → MB Wandler → I/O Port Pin 27
 Memory Switch → MB

Stecker ANIN auf Platine I/O

1 }
 2 } GND
 3 }
 4 }
 5 CV input (Extern CV)
 6
 7 A
 8 D → 4051 Ch.
 9 C
 10 B
 11 S → 4051 Ch.
 12 Tune C.V.
 13
 14 } +5V
 15 }
 16 CV out von 4051

Keyboard Sockel

362 B.

1 6c
 2 6y
 3 6e
 4 6a
 5 6n
 6 63
 7 65
 8 67
 9 66
 10 64
 11 62
 12 68
 13 6n
 14 63
 15 65
 16 67

Abfrage = PIA D
 Ansteuerung = PIA A

- 1 } + 12
- 2 }
- 3 } Analog QND
- 4 }
- 5 } - 12V
- 6 }
- 7 BD3X
- 8 BD2X
- 9 BD8X
- 10 BD6X
- 11 20V4
- 12 BD2
- 13 BD43 - Tot RAM - R/W, Mux - disall
- 14 CV. out
- 15
- 16 Pitch Bend
- 17
- 18 A
- 19 - $\phi x = 2MHz$
- 20 - IRQ - X
- 21 - NMI

BB8x → Platine Dig.

P in
MUX 1
MUX 2
Data 8x
VCF C.V.
VCA C.V.
CS Timer
CS PIA
Res C.V. A
" " B
B2
RW

BB28 PWN B
1 1
2 2
3 3
4 4
5 5
6 6
7 7

AB
AN

BB38 OF0
34 OF1
38 OF2
3C OF3
Timer

BB40 OF0
44 OF1
48 OF2
4C OF3
PIA's

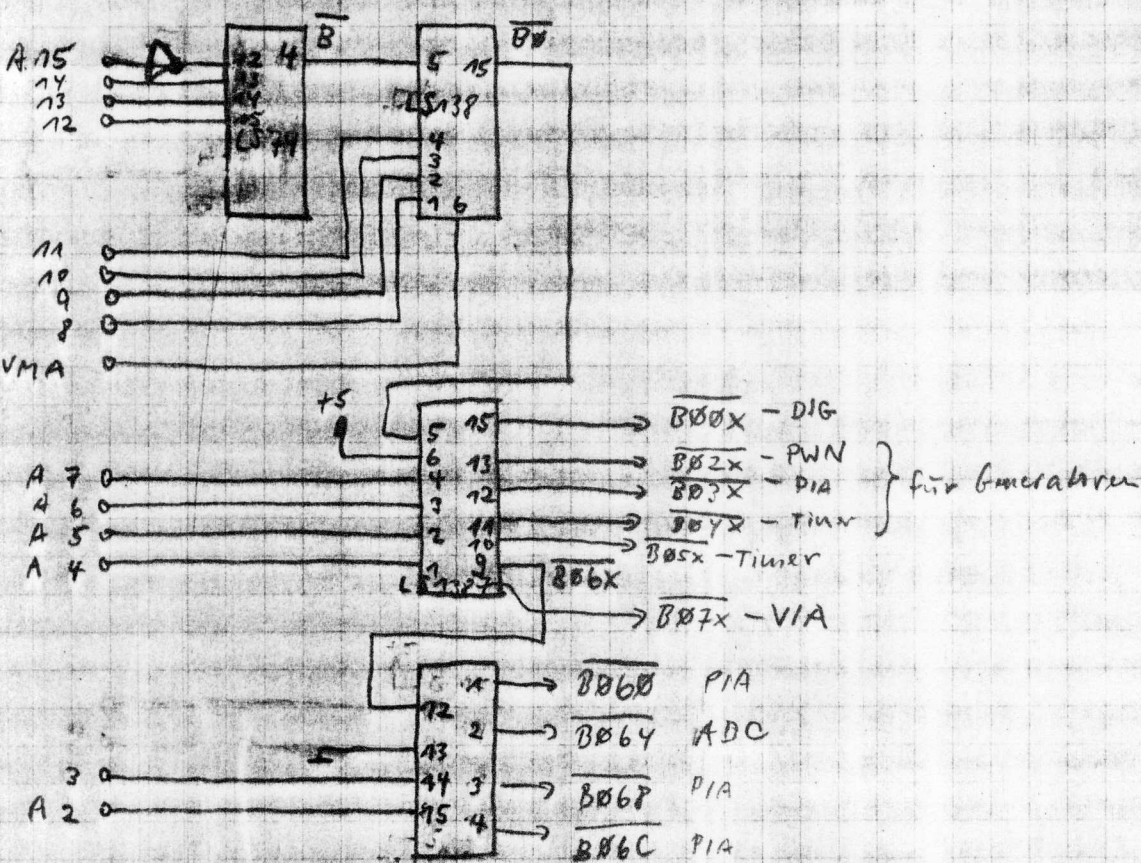
BB58 BIT
BB60 A = Keyb. Ansteuer
BB62 B = Keyb. Aufprall
BB64 A/D Converter, SC
BB66 A = A/D-Converter
BB68 B = DAC 2x Res. Calib
BB6C A = DAC C.V. VCF
BB6E B = DAC C.V. VCA
BB70 A = EXTERN.
BB72 B = Control's, Carrett, Ton, RAM, A/D-Conv.

VIA QHN

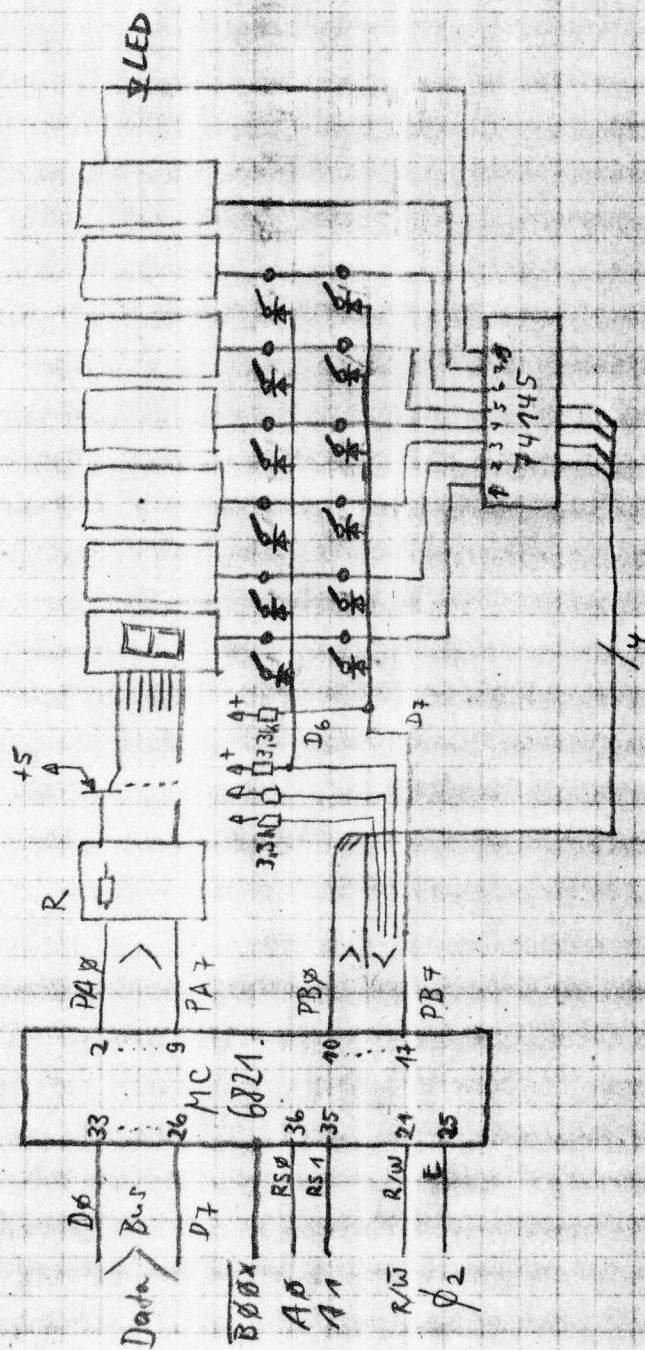
Stecker Platine I/O Gen

Stecker	Platine	I/O Gen
1	+12	Res A C.V.
2		Res B C.V.
3	GND	f in
4		AN
5		AB
6	-12V	VCF C.V.
7	BB3X	VCA C.V.
8	BB4X	MUX B
9	BB5X	MUX A
10	Carrett. Clock out	D0
11	Dyn - f in	1
12	PIA → Ton RAM 1	2
13	PIA → Ton RAM 2	3
14	Res A BB64	4
15	Res B	5
16	Pids. Band	6
17	C.V. VCF	D 7
18	C.V. VCA	Timer Enable BB3X
19	F0 - Ton	P2
20		PIA Enable BB4X
21		R/W. p
22		
23	C.V. input	
24		
25		
26	GND - Extr. C.V. input	
27	Carrett. Data I/O	
28	Trigger out VIA B 64	
29	Trigger in VIA B 63	
30	Trigger In VIA B 62	
31	GND - Extr. C.V. input	

Adressdecodierung auf Platine 1-0 360 B



Digital I/O Board

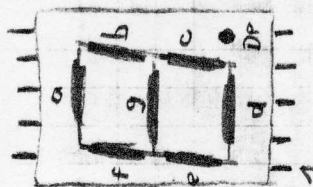


CAY 91 K

Segm.

Pin

Bus



Segm.	Pin	Bus
a	7	D0
b	6	1
c	4	2
d	2	3
e	1	4
f	9	5
DP	10	6
	5	7

Stecker / Flachkabel

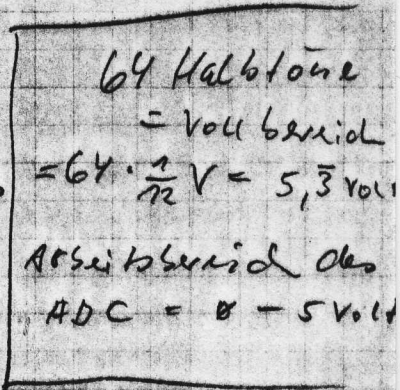
Pin	Stecker / Flachkabel
1 = D0	9 AD
2	10 A1
3	11 A2
4	12 R/W
5	13 800X
6	14 GND
7	15 02
8 = D7	16 +5V

PER Platine

	Bereich	BUS-Steck.	CPU 6802	PIA 6821	PTM 6840	ACIA 6850
Adressen	A0	1	9			
	A1	2	10			
	A2	3	11			
	A3	4	12			
	A4	5	13			
	A5	6	14			
	A6	7	15			
	A7	8	16			
	A8	9	17			
	A9	10	18			
	A10	11	19			
	A11	12	20			
	A12	13	22			
	A13	14	23			
	A14	15	24			
Daten	D0	17	33	33	25	22
	D1	18	32	32	24	21
	D2	19	31	31	23	20
	D3	20	30	30	22	19
	D4	21	29	29	21	18
	D5	22	28	28	20	17
	D6	23	27	27	19	16
	D7	24	26	26	18	15
an Funtle ← externer ← CE1. ←	FIRQ	25	5			
	JRQ	26	4	38/37	9	7
	ØZ	27	37	25	17	14
	Reset	28	40	34	8	
	R/W	29	34	27	13	13
	(+5V) VCC	30	8	20	14	
	GND	31	1	1	1	1

37 pol
Stecker

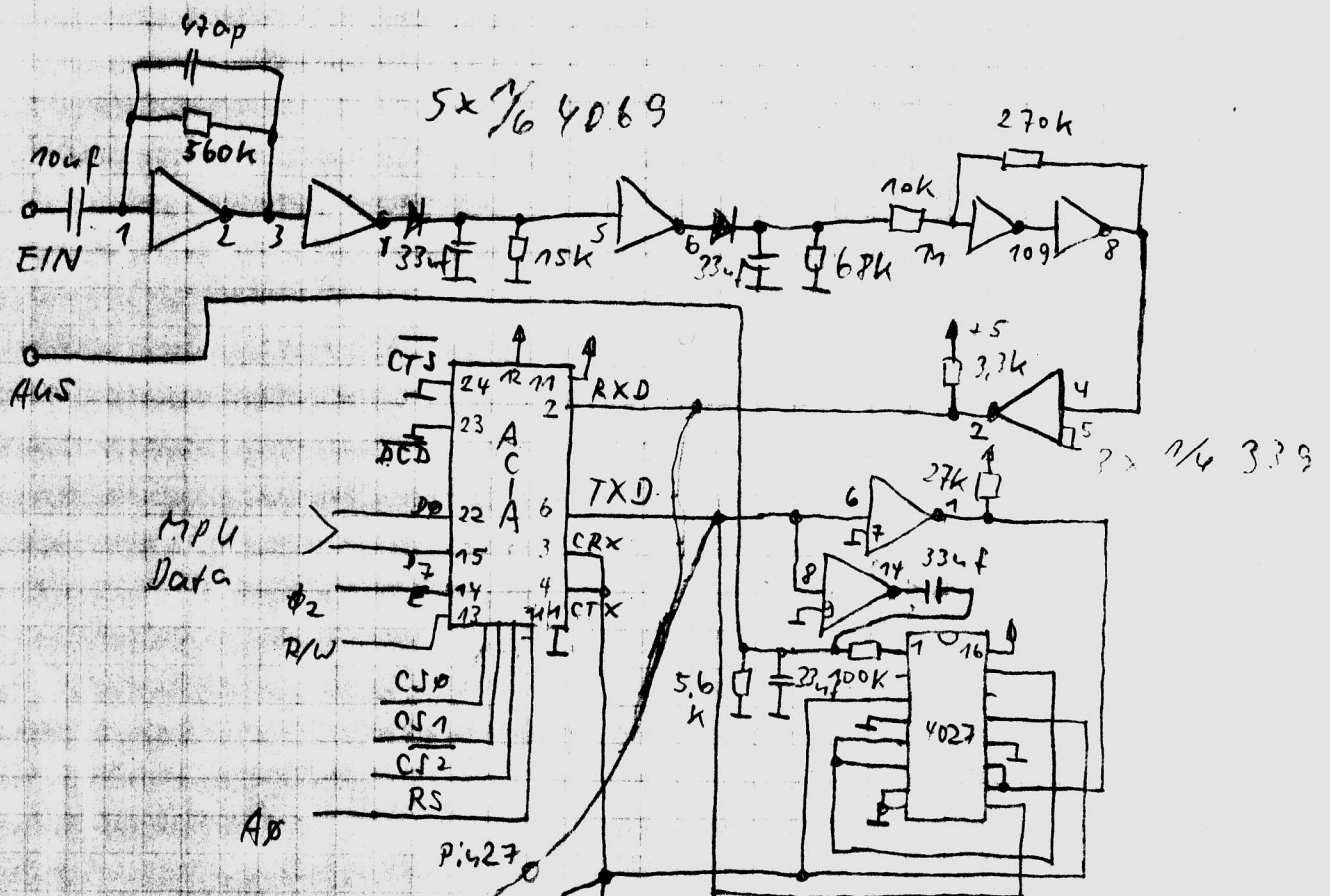
AD-Converter



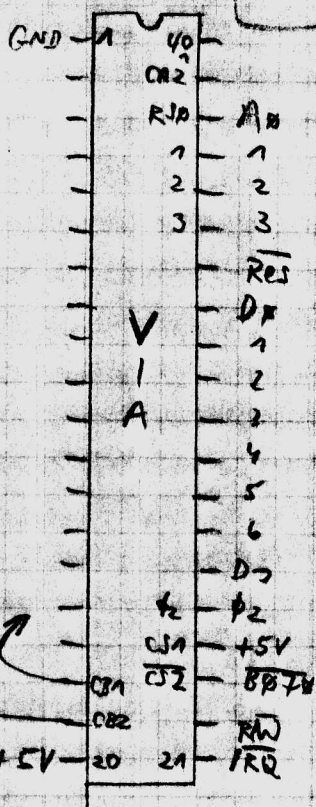
VIA B $\rightarrow$ Flachsteher, Extern⁴

CA 1	9	Handshake
b ₀	10	
b ₁	11	
CA 2	12	
	13	GND
b ₄	14	
b ₅	15	

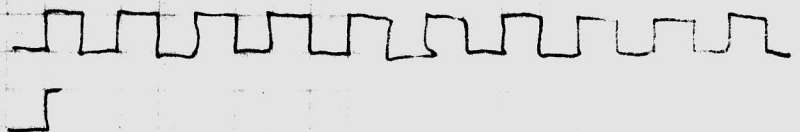
360 - Cassette interface



VIA - CB2
VIA - CB1



Clock



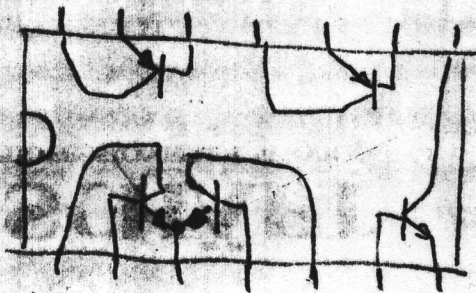
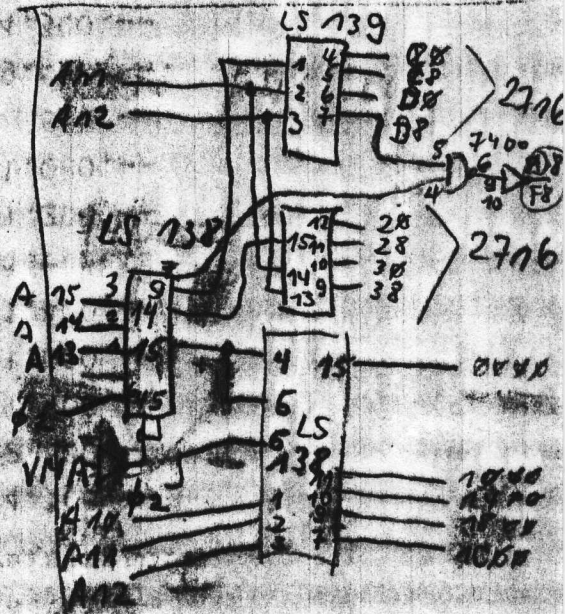
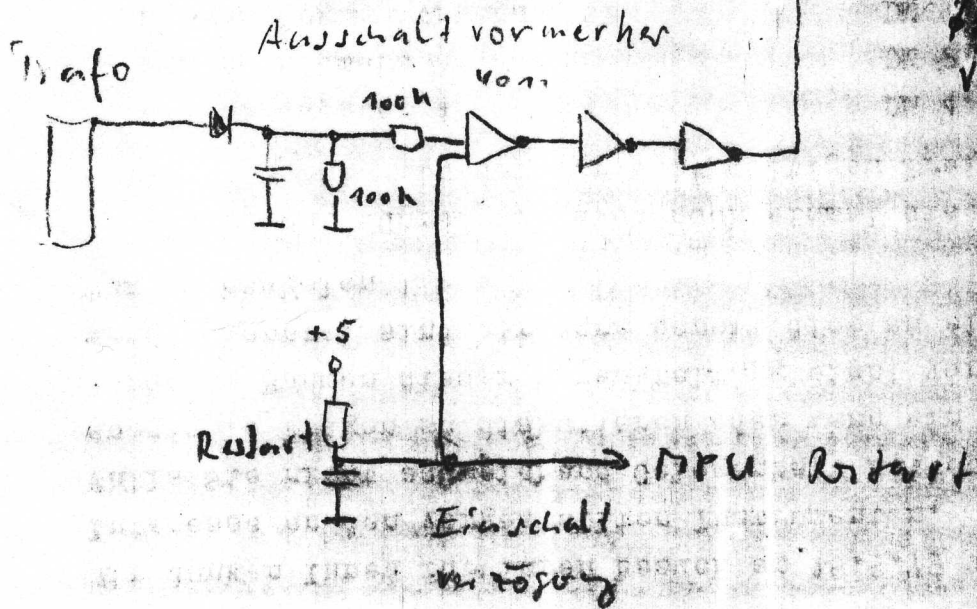
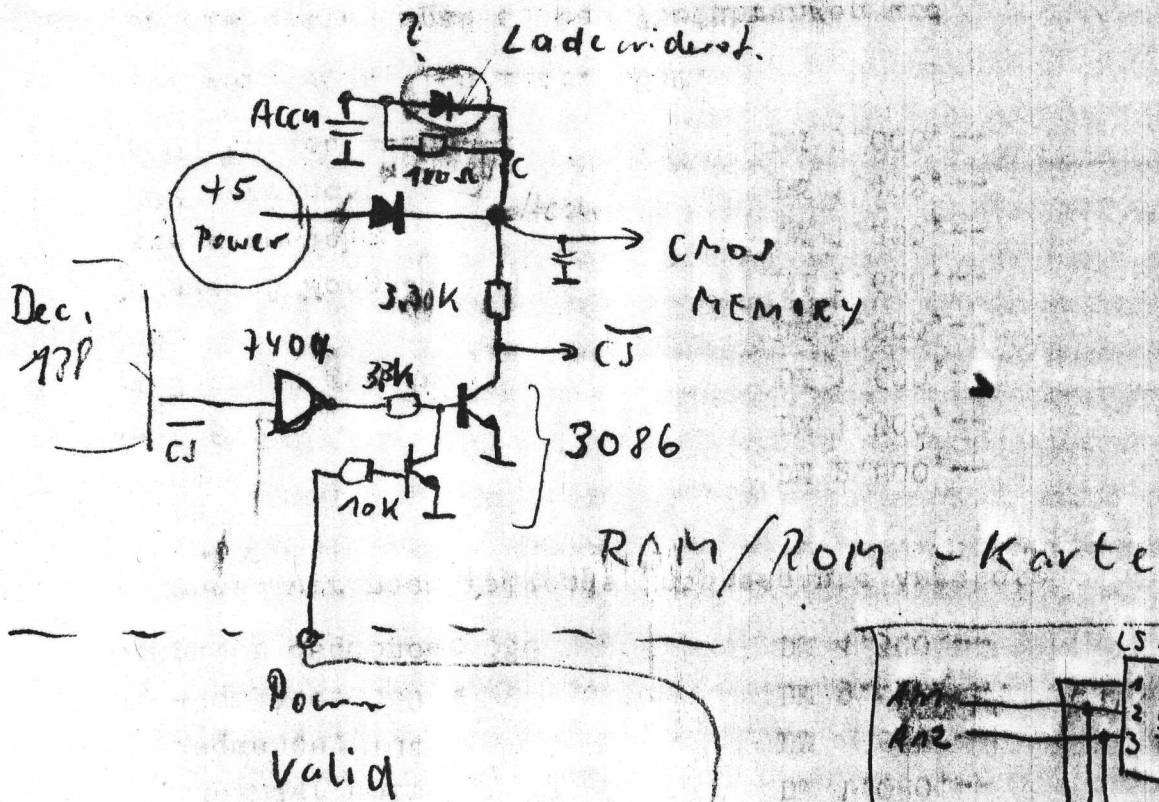
BAUDRATE 300 Bd =

~ 4.5 kHz

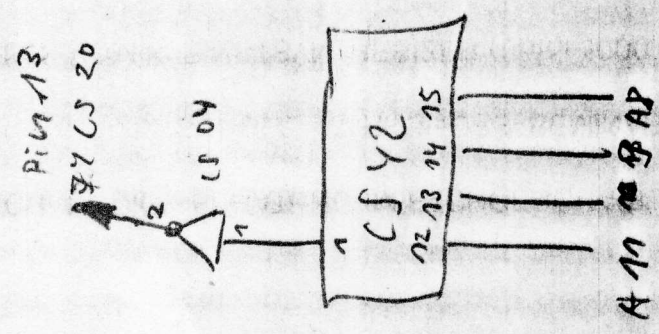
1 MHz = 2²⁰ = 1,048,576

1 MHz = 10⁶ System Clock

360B New RAM/ROM

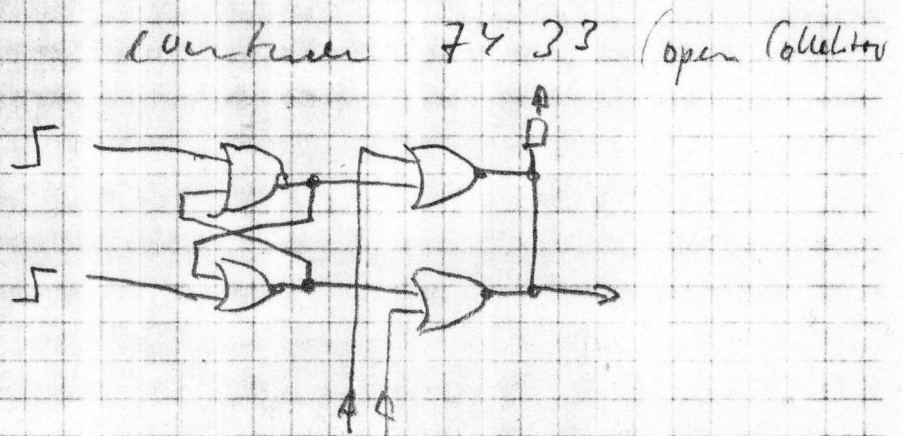
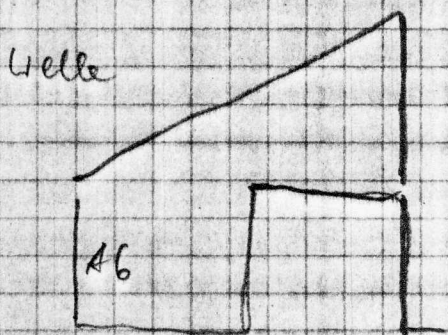
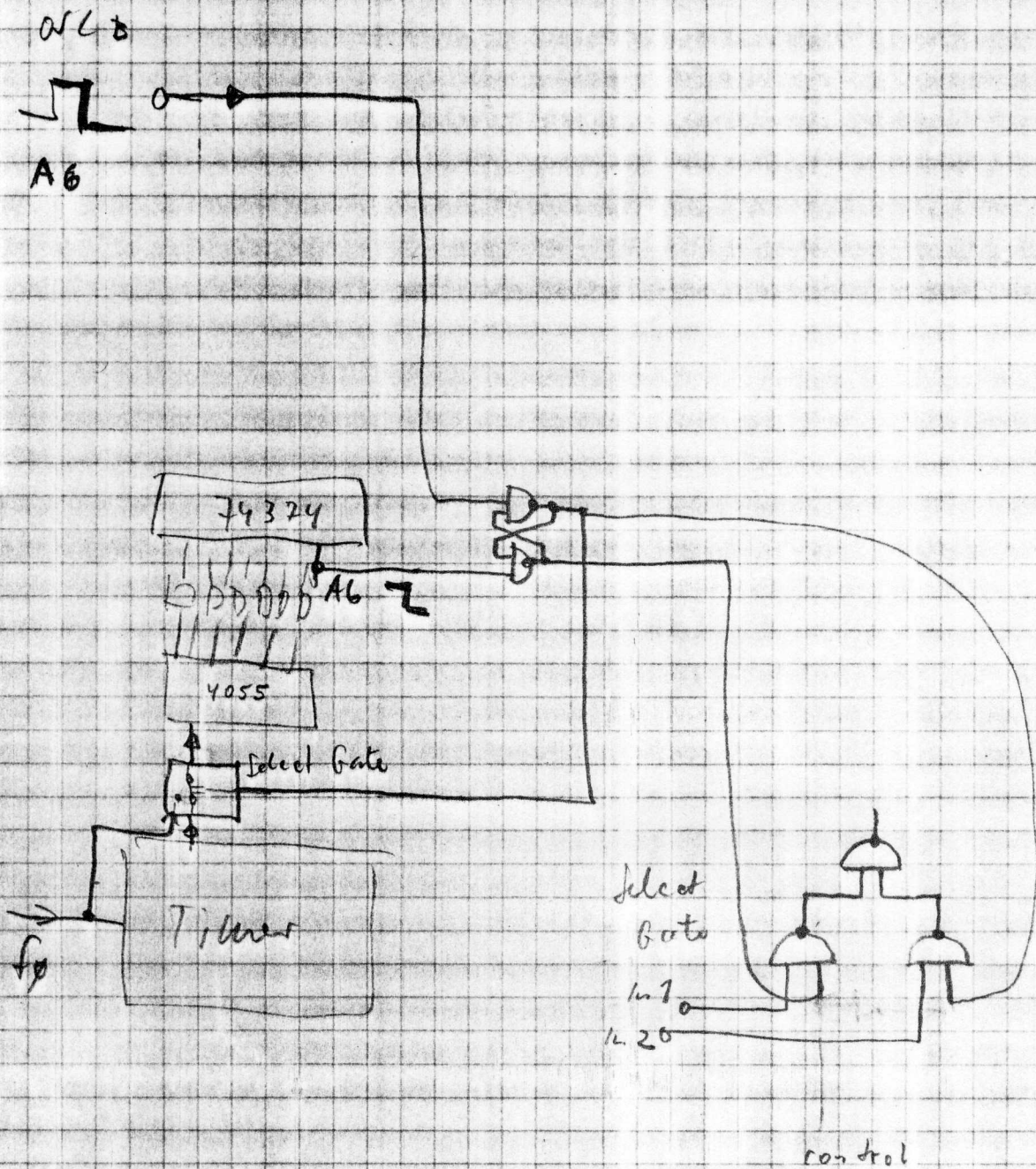


Zusatz zum
 Anschluß an
 340 System
 zur B8xx Selection



360 B

Sync.



PPG 360 - Wave computer

